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VOLUME IV

FTR450262000U

ICAM MANUFACTURING COST/DESIGN GUIDE

ELECTRONICS USER'S MANUAL—VOLUME IV

FINAL TECHNICAL REPORT

1 OCTOBER 1979-31 OCTOBER 1982

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Richard R. Preston

RICHARD R. PRESTON, Capt., USAF
Project Technical Manager
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21 July 1983
Date

FOR THE COMMANDER

N G Tupper

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21 July 83
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Design-to-Cost	Connectors	Integrated Circuits	Soldering
Computer-Aided Manufacturing	Digital Design	Interconnect	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The "Manufacturing Cost/Design Guide" (MC/DG) enables airframe and electronic designers to achieve lowest cost by conducting trade-offs between manufacturing cost and other design factors such as, for electronics, reliability. When fully developed, the MC/DG will permit electronic designers, at all levels of the design process, to quickly perform cost trade comparisons of manufacturing processes and also performance/cost trade-offs on electronics components and subassemblies.

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20. (Continued)

The "MC/DG for Electronics" has two major sections, i.e., for the conceptual design phase and detail design phase. Examples of conceptual design trade-off studies are: standard circuits versus new technology; single assembly versus multiple assembly; identical functions versus shared functions (system partitioning); analog versus digital system design; and impact of built-in test on manufacturing cost. The detail designer-oriented formats include mechanization, processes, insertion (PWA related), soldering (PWA related), and part selection. The formats appear in two forms; firstly, cost-driver effects (CDE) showing the relative impact of cost drivers and, secondly, cost estimating data (CED) providing man-hours or dollars to enable trade-off studies to be conducted.

A feature of the data presented is that the part selection section gives the relative cost for three reliability design levels (commercial and military). The "MC/DG for Electronics" also includes information on manufacturing cost directed to inexperienced designers.

A series of manufacturing cost trade-off study examples are included to indicate the utilization of the conceptual and detail design sections of the "MC/DG for Electronics".

This project is reported in a six-volume Final Technical Report as follows:

VOLUME I. User's Manual - Airframes Volume 1
Contains:
- Utilization Procedures
- Trade-Off Study Examples
- MC/DG Sections for:
  - Sheet Metal
  - Mechanically Fastened Assembly
  - Composites

VOLUME II. User's Manual - Airframes Volume 2
Contains:
- MC/DG Sections for:
  - Extrusions
  - Castings
  - Forgings

VOLUME III. User's Manual - Airframes Volume 3
Contains:
- MC/DG Test, Inspection & Evaluation Section for:
  - Sheet Metal
  - Mechanically Fastened Assembly
  - Castings
  - Forgings
  - Machining
  - Composites

20. (Continued)

VOLUME IV. User's Manual - Electronics Volume 1
Contains:

- Design Process Descriptions;
- Conceptual Design Section for:
  - New Technology
  - Number of Assemblies
  - Common Functions
  - Digital Design
  - Part Count
  - Part Selection
  - -- Package
  - -- Reliability
- Detail Design Section for:
  - Mechanization
  - Processes
  - Insertion Process
  - Soldering Process

VOLUME V. Project Summary

VOLUME VI. Technology Transfer Summary and Report Contents

FOREWORD

This Manufacturing Cost/Design Guide document covers the work performed under Air Force Contract F33615-79-C-5102 from 1 October 1979 through 31 October 1982. The contract is sponsored by the Computer Integrated Manufacturing Branch, Manufacturing Technology Division, Materials Laboratory, Air Force Wright Aeronautical Laboratories. The ICAM Project Manager is Capt. Richard R. Preston. In previous phases, the following Air Force personnel directed the program; Mr. John R. Williamson, Capt. Dan L. Shunk, and Capt. Steven R. LeClair.

The organization of the program is comprised of a coalition of three participating companies with Battelle's Columbus Laboratories (BCL) as the prime contractor. Mr. Bryan R. Noton is the Program Manager at BCL for this design guide.

The participating industrial organizations that are members of the coalition and the Project Managers at each, are:

Electronic Company Subcontractors	Project Managers
Honeywell, Incorporated, Avionics Division	R. Remski
Lockheed-California Company	J. F. Workman
Rockwell International Corporation, Avionics & Missiles Group, Collins Avionics Division	J. G. Vecellio

The participants at each subcontractor company are listed on the following pages.

Note that the number and date in the upper right corner of each page of this document indicates that the document has been prepared according to ICAM's Configuration Management Life-Cycle Documentation requirements for Configuration ITEMS (CIs).

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G. W. Niotta, Avionics - Parts and Equipment	(C)
James R. Saunders, Producibility Cost Analyst, Sr.	(C)

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SECTION 1
INTRODUCTION

1.1 Scope

With its step-by-step approach to attaining the optimum performance at minimum cost, this "Manufacturing Cost/Design Guide" (MC/DG) for Electronics is a tool developed expressly for designers. The approach is the same as that used in the MC/DG for Airframes, which met a long-standing need for such a guide. The Guide's easy-to-use formats provide manufacturing cost data developed from industry-wide practice that allow the user (design, manufacturing, and procurement personnel) to quickly and confidently make the trade-offs necessary to achieve lowest acquisition cost. During the design phase, designers with different levels of experience can conduct simple trade-offs between, for example, manufacturing cost and reliability of electronic parts and assemblies. The MC/DG also establishes data at a level that complements and is conducive to computer-aided design and manufacturing systems.

The "MC/DG for Electronics" was developed by identifying manufacturing cost drivers, data requirements, and conceptual format designs. Designer-oriented formats for conventional and emerging technologies, and for meeting specified criteria were prepared. MC/DG sections were developed for procured items, detail fabrication, assembly, and test, inspection, and evaluation (TI&E) of electronics.

To meet the pressure that exists to recognize manufacturing cost even at the early design phase, MC/DG formats cover the cost impacts of new technologies, part count, number of assemblies, commonality, and digital design that must be evaluated early in the electronic system design phase. Trade-off study examples that instruct conceptual designers in each of these important areas are included. The examples require consideration of system design parameters such as reliability, maintainability, test cost, and vulnerability levels. A conceptual design section gives designers guidance on the cost impact of packaging and of various commercial and military specification requirements to achieve required reliability levels. Finally, the "MC/DG for Electronics" provides manufacturing cost guidance for the detail design phase, covering mechanization, processes, and insertion and soldering of capacitors, coils, diodes, integrated circuits, switches, etc.

As part of this project, it was decided to examine the applicability of the MC/DG data and format development methodologies to built-in test (BIT). The contemporary approach to test, by both DoD and commercial customers, is to require that BIT features be included in the design of new electronic systems. These features allow product failures to be quickly and reliably detected and isolated to a single replaceable unit. The applicability of the MC/DG methodologies to the development of BIT

can provide significant cost reduction opportunities for future systems. A trade-off study has therefore explored various levels of BIT within a line replaceable unit (LRU). The results from the pilot study confirmed that the approach would be of great future importance for developing and expanding MC/DG data and formats for use by conceptual and detail designers on BIT applications to:

- Engineering tests
- Qualification tests
- Burn-in tests
- Fault Isolation to Line Replaceable Unit (LRU)
- Fault Isolation to Shop Replaceable Unit (SRU)
- Maintenance tests.

Table 1-1 provides examples of cost areas that relate to manufacturing concerns and on which the designer of electronics requires information. This table is included here as it was prepared to provide the initial guidance for the designer-oriented formats required in the "MC/DG for Electronics". However, reference to the format selection aids, e.g., Figures 1-4 and 1-5, indicates that the range of formats was considerably expanded. Data and formats for the element listed under procured items, detail fabrication, and also assembly are integrated into Sections 4 and 5 of this volume to enable both conceptual and detail designers to conduct trade-offs in these areas.

TABLE 1-1

ELEMENTS OF CONCERN IN MANUFACTURING ELECTRONIC SYSTEMS

PROCURED ITEMS	DETAIL FABRICATION	ASSEMBLY	
SCHEMATIC PARTS	METALLICS	MECHANICAL ASSEMBLY	HYBRIDS
INTERCONNECT PARTS	NON-METALLICS	COMPONENT ASSEMBLY (PRE-WAVE AND POST-WAVE)	CHASSIS ASSEMBLY
HARDWARE	SURFACE TREATMENT	CLEANING	FINAL EQUIPMENT ASSEMBLY
FABRICATED PARTS	COATINGS	SOLDERING	POST-ASSEMBLY PROCESSES
	MARKING	SHEET METAL/ STANDOFF ASSEMBLY (HARD WIRING)	POTTING
		CABLE/WIRE HARNESSS ASSEMBLY	ADHESIVES

1.2 Objectives

The Manufacturing Cost/Design Guide (MC/DG) Study was initiated to further aid in the attainment of the objectives of the Integrated Computer-Aided Manufacturing (ICAM) program.

The ICAM objectives are to:

(1) Reduce aerospace systems cost
(2) Provide leadership to industry
(3) Increase competence in aerospace manufacturing
(4) Provide for ICAM technology transfer
(5) Improve the USAF's mobilization position
(6) Demonstrate the capability for a totally integrated manufacturing system.

The project objectives are directed at reducing the cost of airframes and electronics. The specific objectives include:

(1) Provide to designers urgently needed, quick, simple, qualitative and quantitative cost comparisons of manufacturing processes
(2) Emphasize design orientation of MC/DG formats and manufacturing man-hour data for use at all phases of the design process, i.e., preliminary and detail design, therefore increasing emphasis on cost as a vital design parameter
(3) Enable more extensive manufacturing cost trade-offs to be conducted on airframe components and aerospace electronics fabrication and assembly
(4) Emphasize potential cost advantages of emerging materials and manufacturing methods, accelerating the transfer of these technologies to production hardware
(5) Guide the designer to the lowest cost manufacturing process early in the design phase
(6) Identify cost-driving manufacturing operational sequences, which provide targets for future computer-aided manufacturing (CAM) efforts.

The importance of early decisions to reduce cost at various stages during the electronic design process is shown in Figure 1-1. The interaction between design and other disciplines is shown in Figure 1-2. In an effort to achieve minimum cost, the performance of the designer is evaluated on the factors shown in Figure 1-3.

To provide an overview of the MC/DG sections and contents, overview selection aids are shown in Figures 1-4 and 1-5.

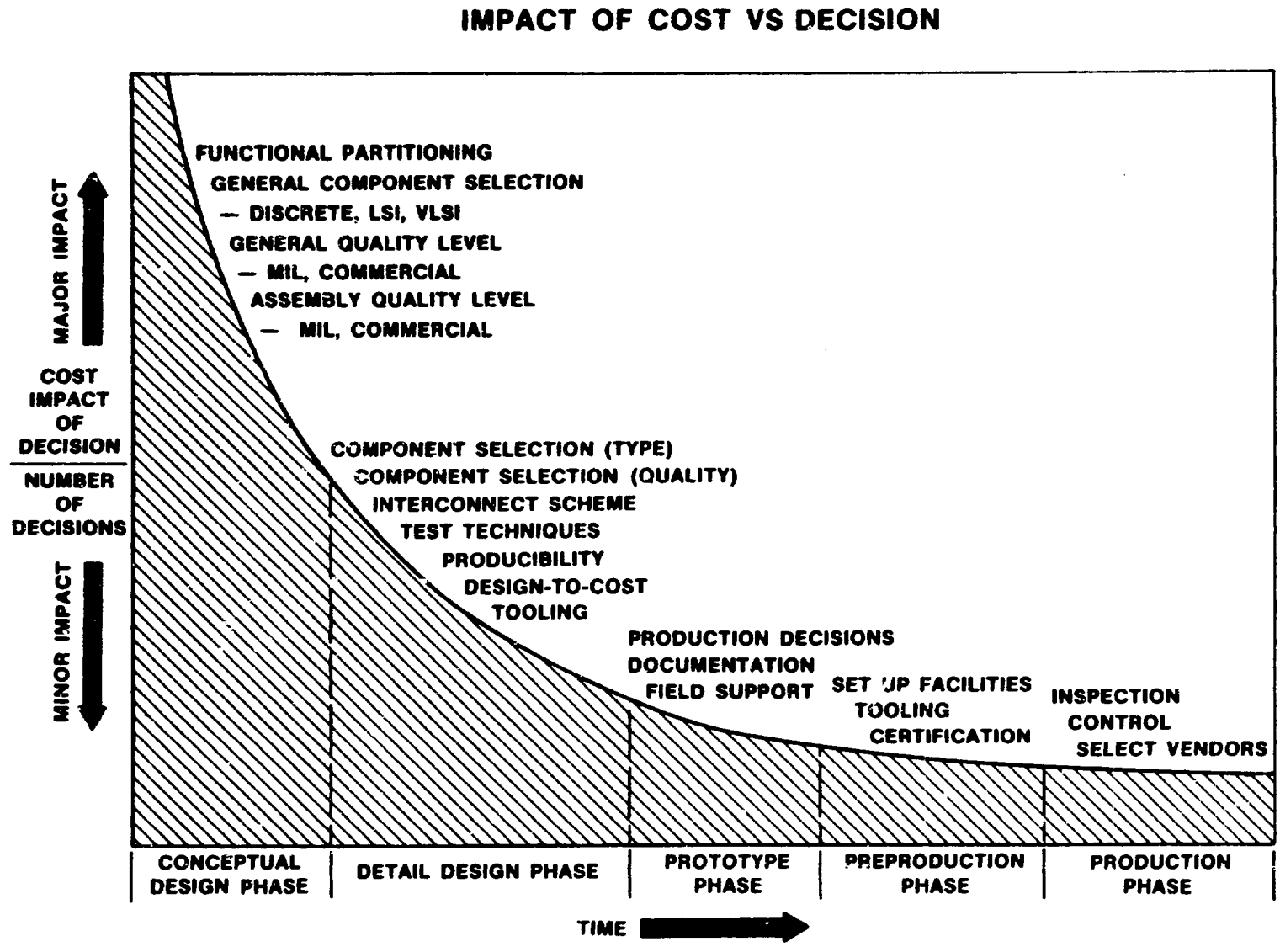

FIGURE 1-1. EARLY DECISION IMPACT CHART

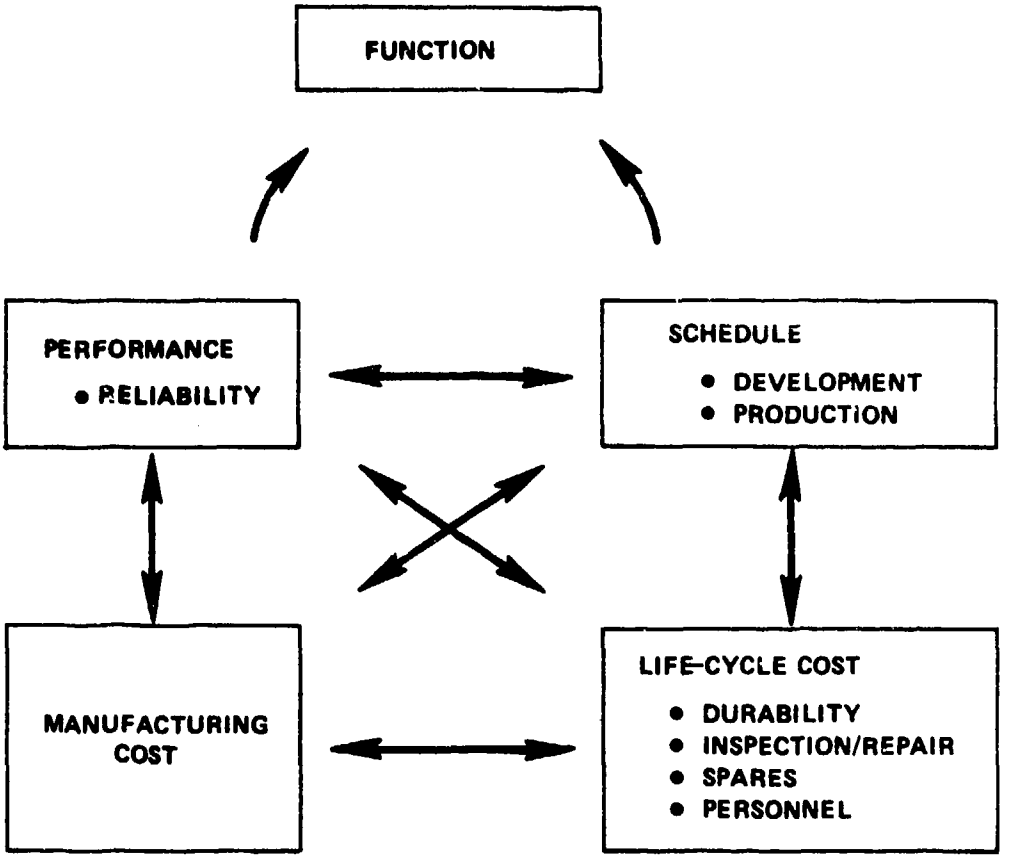

FIGURE 1-2. INTERACTIONS BETWEEN DESIGN AND OTHER DISCIPLINES

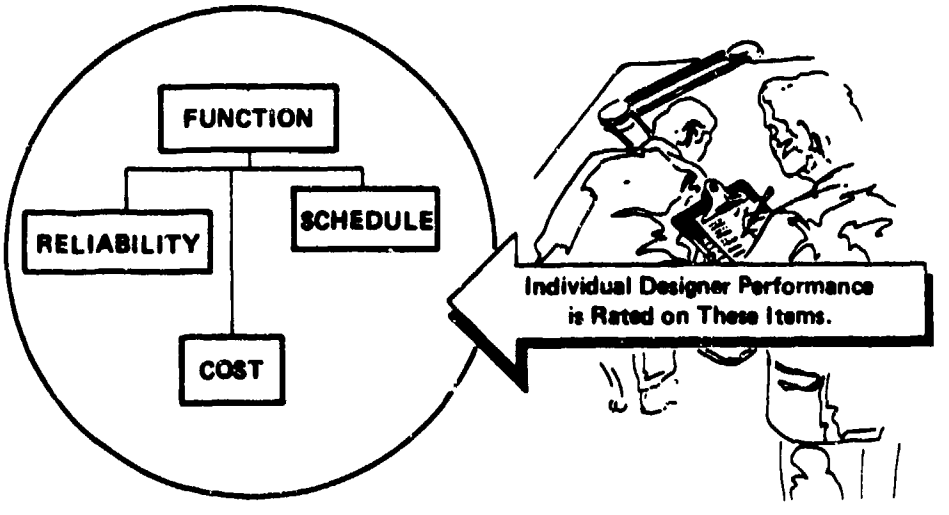

FIGURE 1-3. PRESENT AIRCRAFT DESIGN TEAM PRIORITIES

CONCEPTUAL DESIGN (CD)
FORMAT SELECTION AID

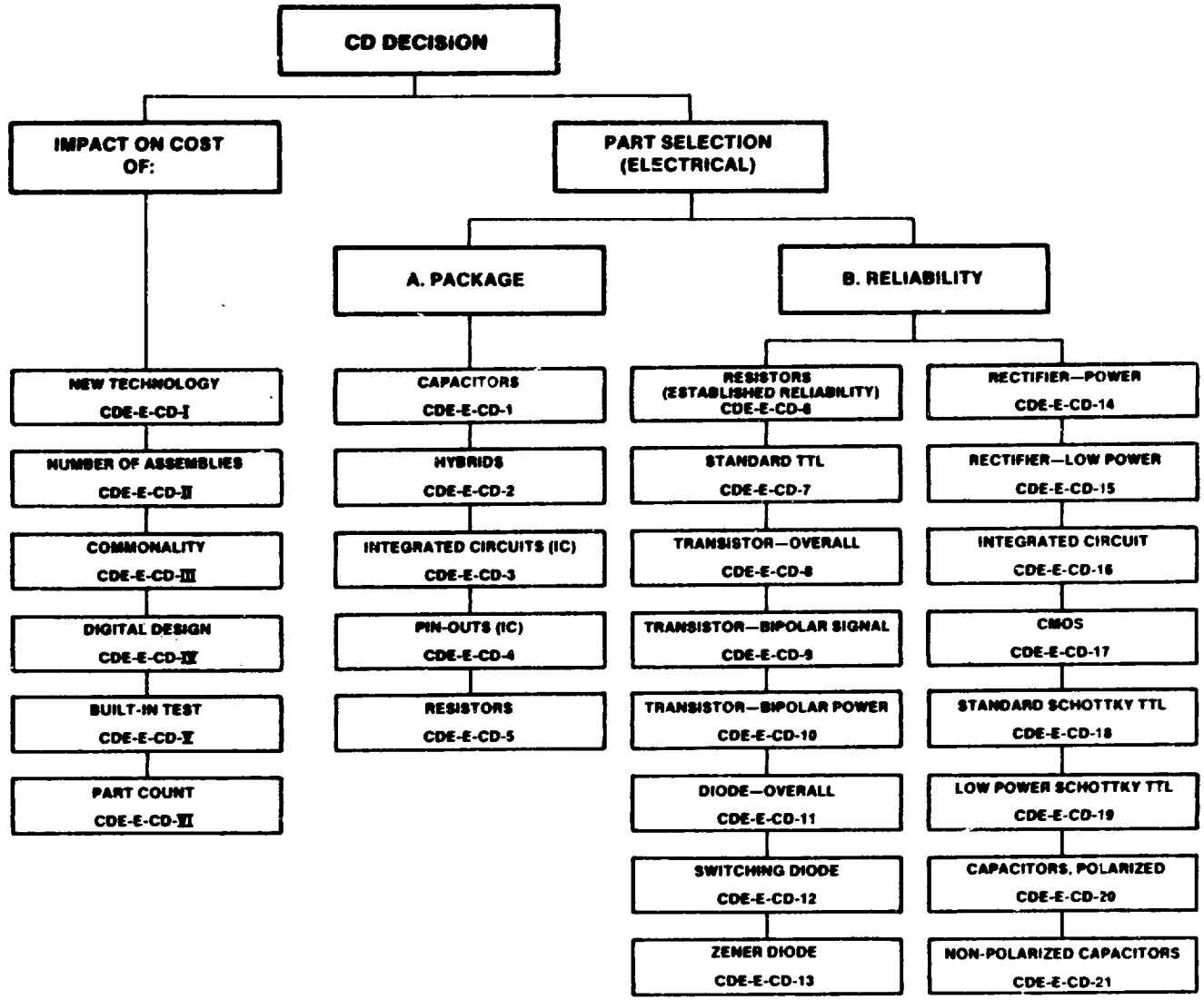

FIGURE 1-4. OVERVIEW SELECTION AID FOR CONCEPTUAL DESIGN (CD)

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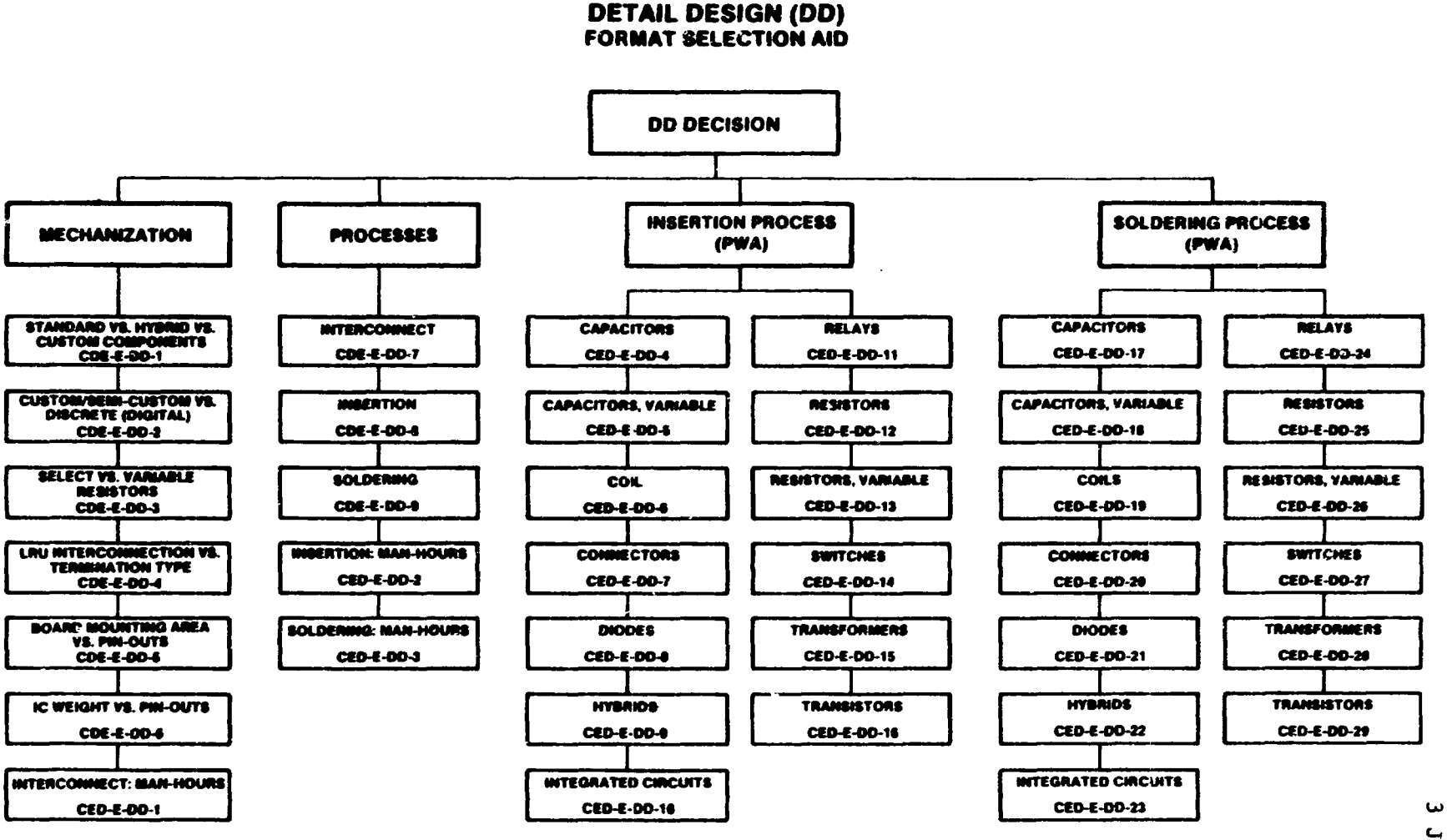

FIGURE 1-5. OVERVIEW SELECTION AID FOR DETAIL DESIGN (DD)

1.3 Designer-Oriented Format Design Criteria

The formats and methodologies developed for the MC/DG concept (AFML-TR-76-227) were used as the basis for format development in the MC/DG for Electronics Fabrication, Assembly, and Test, Inspection, and Evaluation (TI&E). Each project manager in industry was responsible for having the following categories of persons review the data requirements and formats:

- Management (concurrence necessary to assure MC/DG utilization, i.e., achieve technology transfer)
- Engineering (design and support)
- Manufacturing (fabrication, tooling, and quality control)
- Procurement (materials, parts, and equipment).

Furthermore, designer surveys of the MC/DG resulted in the following feedback:

- Must be simple whenever possible
- Must not be time-consuming to use in the design process
- Complicated calculations should be avoided
- Manufacturing data are urgently needed but with designer orientation
- No single electronic company can provide all manufacturing cost data required due to varying expertise
- Designers are more concerned that it is the lowest cost rather than what it costs, i.e., qualitative comparisons are important.

It was agreed that the MC/DG formats must meet the following criteria:

- Emphasize cost drivers
- Be simple to use
- Use designer language
- Instill confidence
- Be economical
- Be accessible
- Be maintainable.

The following is a detailed explanation of the format development criteria.

1.3.1 Emphasize Cost Drivers

The MC/DG will emphasize sensitive factors, which by minor variation in selection can cause major increases or decreases in manufacturing cost. The degree of impact on manufacturing cost during the design, developed through the selection of materials, manufacturing, and fabrication processes, must be depicted in formats and data that will make the designer readily aware of those elements of design (cost drivers) that pose manufacturing cost hazards.

1.3.2 Be Simple to Use

The Cost-Driver Effects (CDE) and Cost Estimating Data (CED) formats used to guide designers will require little or no arithmetical calculations to determine the cost comparisons of design/manufacturing alternatives. The cost impact formats and graphics will provide more direct readout of man-hours through maximum use of simple curves and tables.

1.3.3 Use Designer Language

The primary purpose of the MC/DG is to display manufacturing process capabilities and costs in a manner that will permit designers to select the most economical manufacturing approach. The formats must be developed through a close working relationship with design personnel at all the team member companies and through constructive recommendations submitted during the development of the MC/DG. The charts and terminology included with the formats must be common to the engineering community and be of the types which are recognized and employed by the designer in his daily engineering tasks.

1.3.4 Instill Confidence

The designer must have a high degree of confidence in the CDE and CED formats and manufacturing man-hour data if the MC/DG is to serve as a useful working tool for design. The formats developed will be related to practical and meaningful cost trades that are illustrative of the everyday airframe design decisions made by designers. The formats must clearly provide an MC/DG for making trade-off decisions between manufacturing technologies with both comparative and quantitative cost data. It is recognized that the degree of accuracy of manufacturing man-hour data integrated into the formats will be a significant factor in determinating the confidence and degree of utilization of the MC/DG in industry.

1.3.5 Be Economical

High priority must be given to minimizing acquisition and maintenance costs of the data and formats.

1.3.6 Be Accessible

The MC/DG must be readily available at all designer locations. This will be handled differently within each company, but along similar lines. Copies of the MC/DG can be issued to individual designers or small engineering groups. The wider the distribution of the MC/DG to individual users, the more extensive use can be expected. The breadth and distribution should be weighted between the ease of access by individual designers and the cost of distribution. Computerization will greatly enhance the accessibility.

1.3.7 Be Maintainable

The formats must be developed to facilitate maintenance of the MC/DG. In today's highly fluid technical and economic environment, the useful life

of the MC/DG will depend upon the flexibility of the formats to accept revised or new data. One approach is through computer preparation of individual pages of loose-leaf-type volumes. The data would be stored in the central data bank and, for user accessibility, transmitted via telephone connections to remote terminals at each company for printout and multiple distribution. This is discussed in Volume III of report number AFWAL-TR-80-4115 dealing with MC/DG computerization.

1.4 Data Presentation Methodologies

Throughout the presentations of MC/DG data requirements and formats, the following two terminologies are frequently used:

COST-DRIVER EFFECTS (CDE)

COST ESTIMATING DATA (CED).

The objectives of the CDE and CED methodologies are:

• To develop a simple approach for the use of formatted data by designers to achieve lower fabrication costs during design phases; both CDE and CED.	DIRECTION
• To provide qualitative cost guidance to perform simple trade-offs to achieve lowest fabrication cost; CDE.	COMPARISON
• To provide the designer with the capability to perform simple trade-offs to achieve quantitative rough-order-of magnitude (ROM) estimated fabrication costs; CED.	COST

The CDE and CED methodologies provide the designer with cost guidance for achieving lower manufacturing costs at the preliminary detailed design phase:

CDE achieves qualitative results.

CED provides quantitative results.

The CDE approach enables preliminary and production designers to:

- Identify the intensive cost drivers that increase the manufacturing cost of the design
- Determine the relative cost effects of cost drivers over which they have control
- Determine pertinent cost data that allow them to perform simple trade-offs leading to comparative costs for those configurations evaluated.

The CDE approach motivates designers. They can obtain low cost designs, providing they take full advantage of the CDE data and use the lower end of the cost range wherever possible, while satisfying the performance and reliability requirements.

The CED approach provides preliminary and detail designers with the ability to perform cost estimates through the use of simplified formats and data. CED values are both quantitative and comparative.

1.5 Data Generation

1.5.1 Recurring Costs

Throughout the MC/DG, team average production man-hours are given. Direct material costs are not included. The direct factory labor costs for manufacturing base parts and designer-influenced cost elements (DICE) were generated by the participating aerospace companies using their own time standards, excluding personal fatigue and delay (PF&D) allowances. In developing data for recurring costs for base parts and DICE, general and detailed ground rules were formulated by the coalition to assure consistent results. Elements that affect the costs, such as lot release, program quantity, and learning curves, were included in the generation of data.

Direct factory labor recurring costs consist of setup (SU) time and run time. The SU time is that time required to prepare for a production operation and is required once for each lot of parts to be manufactured.

The production run time is that time required to produce a single part for storage or use in assembly. The direct factory labor time per part is obtained by dividing the SU time by the lot size, e.g., 25, as an industry average, and then adding the run time per part.

1.5.2 Nonrecurring Tooling Costs (NRTC)

Standard tools are used, when available, to fabricate the base part and to incorporate the DICE. NRTC is recorded in man-hours.

SECTION 2
REFERENCES/GLOSSARY

2.1 Applicable Documents

Item	Description
1	Integrated Computer Aided Manufacturing (ICAM) "Manufacturing Cost/Design Guide" (MC/DG) Interim Technical Reports for Period: a. 28 September 1979 - 28 February 1980, ITR4502600001U b. 1 March 1980 - 16 May 1980, ITR4502600002U c. 17 May 1980 - 16 July 1980, ITR4502600003U d. 17 July 1980 - 31 October 1980, ITR4502600004U e. 1 November 1980 - 30 January 1981, ITR4502600005U f. 31 January 1981 - 30 April 1981, ITR4502600006U g. 1 May 1981 - 31 July 1981, ITR4502600007U h. 1 August 1981 - 30 October 1981, ITR4502600008U i. 31 October 1981 - 29 January 1982, ITR4502600009U.
2	Summary Report on the Air Force/Industry Electronics Manufacturing Cost Reduction Study, Air Force Materials Laboratory, AFML-TM-LT-75-2, 24-29 March 1974.
3	Noton, B. R., et al, "Manufacturing Cost/Design Guide", Materials Laboratory, Air Force Wright Aeronautical Laboratories, Wright-Patterson Air Force Base, Ohio. Technical Report AFML-TR-76-227, December 1976.
4	Test Methods and Procedures for Microelectronics, MIL-STD-883B, 31 August 1977.
5	Noton, B. R., Claydon, C. R., Larson, M., "ICAM Manufacturing Cost/Design Guide", Materials Laboratory, Air Force Wright Aeronautical Laboratories, Wright-Patterson Air Force Base, Ohio. Technical Report AFWAL-TR-80-4115, September 1977 - July 1979 a. Volume I: Demonstration Sections b. Volume II: Appendices to Demonstration Sections c. Volume III: Computerization.
6	General Specifications for Semi-Conductor Devices, MIL-S-19500, 28 November 1978.
7	Reliability Prediction of Electronic Equipment, MIL-HDBK-217C, 9 April 1979.
8	General Specifications for Microcircuits, MIL-M-38510, 1 December 1981.
9	Reliability Prediction of Electronic Equipment, MIL-HDBK-217D, 15 January 1982.

2.2 Terms and Abbreviations

2.2.1 Glossary for Electronics Fabrication and Assembly

AI: Auto-Insert.

ATE: Automatic Test Equipment.

AWG: American Wire Gauge.

Base Part: A component or part at its simplest functional level.

Canned: A packaging technique for integrated circuits, hybrids, and transistors which resembles a "can".

CMOS: Complementary Metal-Oxide Semiconductor.

Component: Purchased and fabricated electronic parts.

Component Selection: Performed by the component applications and standards group. Procedure begins with (1) designer recommendations, (2) concurrence by reliability engineering, (3) concurrence by standards engineering, and finally with (4) purchasing. Recommends alternatives of generic types based on price.

Density: Discrete parts per unit area ($in.^2$).

Designer: A person responsible for the creation of an electronic assembly. This responsibility encompasses systems, electronics, and mechanical engineering.

Designer-Influenced Cost Elements (DICE): Those elements that add cost to base part configuration. Included might be tolerances, procedures, reliability requirements, and special test requirements.

DIP: Dual In-Line Package.

Discrete Part: A component, part, or lower assembly, such as printed wiring board, heat sink, wire, substrate, or electronic component ready for assembly; i.e., a base part with DICE. A discrete part may, in some cases, be a subassembly.

Electronic Assembly: A group of discrete parts joined together and tested.

Electronic Part Selection: Performed by the designer based on a standard parts catalogue with assistance from the Applications and Reliability Engineering Functions.

Emerging Manufacturing Methods: Those methods that are not currently used in manufacturing but will be standard processes within the next 5 to 10 years.

Environmental Impact: Effects of a device or system on the environment in the vehicle mounting location area, or effects of vehicle mounting location environment on hardware being evaluated.

Failure Rate: Number of predicted failures per 1,000,000 hours in accordance with MIL-Std.-217C.

Flatpack: A packaging technique for integrated circuits.

Hybrid: Electronic package usually containing several LSI's, discrete resistors, capacitors, and transistors.

Indenture: Hardware level within the total system, i.e., system, LRU, or SRU.

IR: Infrared.

JAN: Joint Army-Navy.

JANTX: Piece part reliability level - extra testing (100%).

JANTXV: Piece part reliability level - extra testing (100%) visual.

JEDEC: Joint Electron Device Engineering Council.

LRU: Line Replaceable Unit (on operational aircraft).

LSI: Large Scale Integration.

Manufacturing: A series of interrelated activities and operations involving planning, fabrication, assembly, quality assurance, testing, management, and product support.

Material: Any commodity used directly in producing a product (raw materials, component parts, subassemblies).

MIP: Multiple In-Line Package (same as PGA).

MOS: Metal Oxide Semiconductor.

MSI: Medium Scale Integrated Circuit.

PCB: Printed Circuit Board.

PGA: Pin Grid Array.

POT: Potentiometer.

PWA: Printed Wiring Assembly.

PWB: Printed Wiring Board.

Screening: A process that consists of temperature cycling, power cycling, and vibration either concurrently or in a particular sequence to produce infant mortality on electronic parts so that higher reliabilities can be achieved in equipment operation. This process can be completed at the part, subassembly, assembly, or equipment level.

Semi-Auto-Insert: Hand inserted components using a location aid such as templates or illuminated arrows.

Setup Time: The standard hours required to make ready or to prepare for the performance of a job or operation. These hours also include teardown or cleanup efforts.

SIP: Single In-Line Package.

SRU: Shop Replaceable Unit (intermediate maintenance activity in base shop).

SSI: Small-Scale Integrated Circuit.

Standard Hour: The Industrial Engineering Standard Hours to perform a specific manufacturing operation. This does not refer to any specific Industrial Engineering method and time measurement system.

Standard Part: A procured electronic or mechanical part that is approved for use in military avionic designs and has a MIL-Standard slash sheet defined.

T^2L: Transistor-Transistor Logic.

Tool Family:

- Special: The adapter that would be developed to allow interface with an automatic test station or the test fixture that would provide power input and output interface with the assembly to allow standard test equipment to be used. Test points would be made readily available for ease of test.

- Standard: The test equipment required to provide stimulus and measure response of the assembly being tested.

- Shop Aids: Routing boards used by assembly personnel for wiring complex harnesses for interconnect within the equipment.

Tools: In the electronics industry these consist of tools in a mechanical sense (e.g., gauges and fixtures) but also include electronic fixtures necessary for assembly testing (automatic or manual) and software required to test the assembly.

Unique Functions: Dedicated special purpose circuit such as microprocessor (normally I/O circuits).

VHSIC: Very High-Speed Integrated Circuit

VLSI: Very Large-Scale Integrated Circuit.

XTAL: Crystal.

2.2.2 Glossary for Test, Inspection, and Evaluation

Product Assurance: The planned interdisciplinary and systematic establishment and application of all quality assurance, quality control, reliability, and maintainability actions necessary to provide adequate confidence on an independent basis that: requirements are properly specified; the design will achieve these requirements; adequate test, inspection, and evaluation systems are established to detect nonconformance; and the final product will perform the intended function(s) in the operational environment for the designed life cycle.

Quality: The composite of all the attributes or characteristics including performance of an item or product.

Quality Assurance: The planned and systematic establishment of all actions (management/engineering) necessary to provide adequate confidence that nonconformance prevention provisions and reviews are established during the design phase and performed throughout the product manufacturing and life-cycle phases.

Quality Control: The planned and systematic application of all actions (management/technical) necessary to control raw materials or products and detect nonconforming materials or products through the use of test, inspect, evaluate, and audit techniques.

Test, Inspection, and Evaluation (TI&E): TI&E are three techniques utilized to carry out quality control activities. Specific techniques are used to determine whether materials, components, and/or end items conform to specified standards, specifications, and/or requirements. The TI&E techniques are normally addressed with specific detail in the quality control inspection plan or equivalent documents.

SECTION 3
HOW MC/DG IS USED

3.1 Manufacturing Cost/Design Guide Design Process Interaction

Because designers are the primary users of the "Manufacturing Cost/Design Guide" (MC/DG), it is recognized that their needs at different levels dictate the organization, structure, and formats of the guide sections. Therefore, an analysis of the design process was performed in order to relate the interaction of the MC/DG with the design process.

Based on results of this analysis at the team member companies, the generic flow chart for the design process shown in Figure 3-1 was preferred. The design process consists of the following phases:

- Conceptual design phase
  - Pre-proposal study activity
  - Proposal design activity
- Detail design phase
- Design review
- Production release.

The stages at which the MC/DG design formats are utilized are indicated on Figure 3-1. As shown, CDE formats are particularly useful at the proposal or conceptual design phase. The CED formats are especially important for the detail design phase of electronics and, as indicated on the flow diagram, are used for both circuit and mechanical design. Note that the production release is based on the lowest manufacturing cost while meeting the design requirements.

The systems concept formulation requires consideration of a number of important design parameters in electronics, including:

- Reliability ⟶ Goal MTBF
- Maintainability ⟶ Goal MTTR
- Cost ⟶ Cost Bogie or DTC Goal
- Environmental ⟶ Quality Levels - Operational Levels
  - Temperature
  - Vibration
  - Shock
  - Radiation
  - Altitude

TYPICAL DESIGN FLOW FOR AEROSPACE ELECTRONICS INDUSTRY

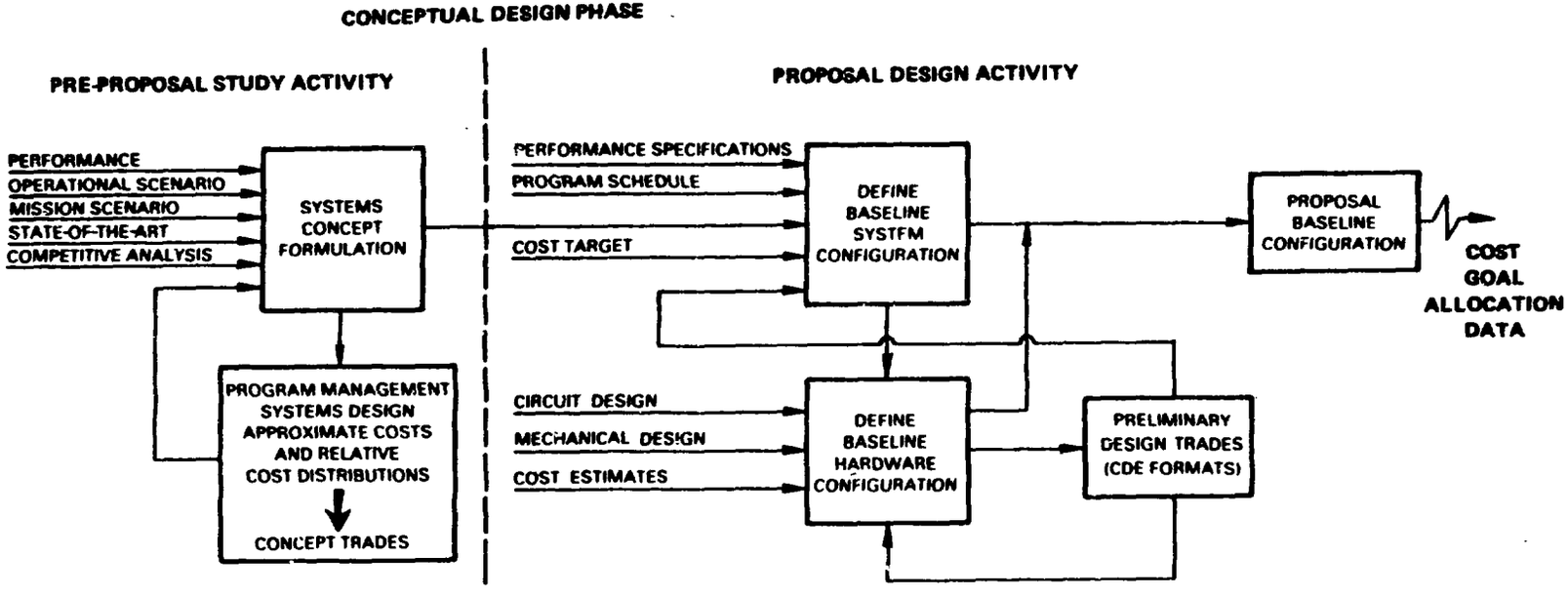

FIGURE 3-1. DESIGN PROCESS FLOW CHART

TYPICAL DESIGN FLOW FOR AEROSPACE ELECTRONICS INDUSTRY (Continued)

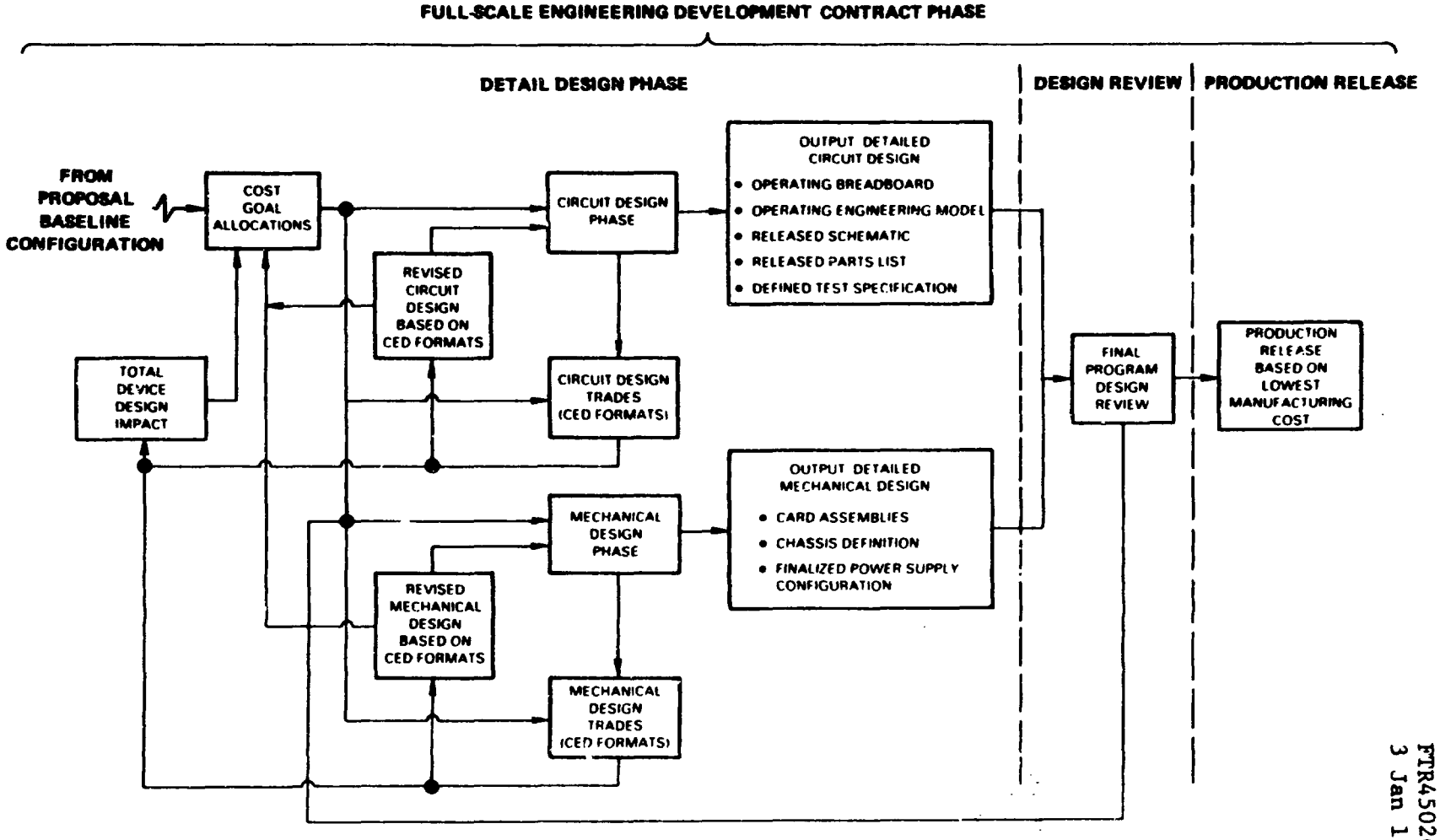

FIGURE 3-1. DESIGN PROCESS FLOW CHART (Continued)

- Operation/Mission Requirements
  - Fault Tolerance
  - Power-on Cycles
  - Mission/Flight Critical.

To realize minimum manufacturing cost, it is necessary for designers of electronic systems to be aware of the cost drivers that must be addressed throughout the development and production. The following design and manufacturing concerns in the development of electronics can have significant cost impact:

- Single source/proprietary items
- Insufficient test points
- Back-to-back card modules
- Shielded wire
- Unique wire gauges
- Solder sleeve terminations
- Solder cup connectors
- Flextape
- Chassis mounted components
- Multilayer printed wiring boards
- Components that cannot be auto-inserted
- Multi-row interface connectors
- Masking, unmasking, and touch-up
- Special tools for insertion or extraction
- Multiple range of fasteners
- Handwiring
- Transformer clearances
- Mil-spec versus commercial components and parts
- Test, inspection, and evaluation (TI&E)
- Shock and anti-vibration mountings (requirement to withstand high "g" impact)
- Wire identification (stamping on wires, sleeving, or color-coded wire)
- RFI shielded cables

- Tolerances (circuit boards, capacitors, resistors, controls, etc.)
- Nonstandard cabinets and racks
- Conventional wire harness versus ribbon harness or printed circuit boards
- Multi-piece racks and boxes
- Silk-screening and engraving on panels versus decals, stampings, etc.

3.2 Trade-Off Study Examples Addressed

Many trade-off studies are required in the development of any complex aerospace electronic system. The following are examples of such trade-off studies:

I. Conceptual Design

A. Standard Circuits versus New Technology

- Cost
- Weight
- Size
- Reliability
- Maintainability
- Probability of Availability
- Factory Handling Capability
- Multiple Source (Candidate Control)

B. Common Functions versus Unique Functions

- Multi-Mode Computational Capability
- Reliability
- Space Availability
- Data Transmission
- Fault Isolation Capability
- Flight/Mission Critical

C. Analog versus Digital Processing

- Interface
  - I/O
  - Required Conversions
- Part Availability
- Part Costs
- Reliability
- Hardware/Software Integration
- Number of Functions
- Operational Definition
- Test Costs

II. Detail Design

A. Adding Cuts/Jumpers versus Redesigning Printed Wiring Board

- Quantity of Cuts and Jumpers
- Cost per Cut and Jumper (Labor)
- Cost of Redesign of PWA
- Volume of Assembly Remaining

B. Soldering: Automatic Wave versus Vapor Phase versus Manual

- Density
- Type of Component
- Type of Lead Form

C. Auto-Insertion versus Hand-Insertion

- Quantity of Assemblies
- Type of Component
- Number of Axes - Component Orientation
- Number of Boards per Blank
- Footprint
- Lot Sizes

3.3 Procedure to Conduct Trade-Offs

Sections 4 and 5 of the "MC/DG for Electronics" provide examples of conceptual and detail design trade-offs, respectively, using the MC/DG formats. The steps to conduct trade-offs in the conceptual and detail design phases are listed below:

Conceptual Design Phase

Step 1. Review customer requirements and applicable specifications.

Step 2. Review general and detailed ground rules in MC/DG.

Step 3. Review format selection chart for design parameters.

Step 4. Specify trade-off to be conducted, i.e., new technology, part count, etc., and prepare conceptual design format, e.g., CDE-E-I.

Step 5. Using data from MC/DG, determine and tabulate values showing cost differentials, i.e., increase or decrease.

Detail Design Phase

Step 1. Review customer requirements and applicable specifications.

Step 2. Review general and detailed ground rules in MC/DG.

Step 3. Define new concept; begin detail design, e.g., printed wiring assembly (PWA) for power supply.

Step 4. Using format selection aid, choose required formats, e.g., impact of select versus variable resistors.

Step 5. Determine material costs for concept, e.g., PWA, using worksheet.

Step 6. Use charts to select parts for the concept based on available technologies.

Step 7. Use labor estimation worksheet to determine labor costs for all concepts.

Step 8. Use designer's cost worksheet to determine cost change from baseline.

Step 9. Prepare summary.

3.4 Cost Worksheet for Electronic Designers

Electronic designers can utilize the MC/DG data and formats in a number of ways. When it is necessary to determine the total cost of an electronic subassembly or assembly, the cost worksheet shown in Table 3-1, can be used at the discretion of the designer. This enables the cost savings or cost increase to be noted in reference to a specified baseline configuration.

TABLE 3-1

MC/DG ELECTRONIC DESIGNER'S COST WORKSHEET

Baseline Configuration:
Indenture Level:

Baseline Manufacturing Cost Allocation: $ _____

DESIGN DECISION: Part Selection	1	2	3	4	5	6	7
Piece Part Type	**% Total Electronic Part Cost**	**Baseline Approach**	**Reference**	**Study Approach**	**Ratio: Baseline to Study Approaches**	**Cost Factor (%) (1 ÷ 5)**	**Cost* Change (%) (1 - 6)**

Total _____

Cost Impact: **Baseline Manufacturing Cost ($) x Cost Change Total (%) = ($)** _____ **x** _____ **(%: Total of Column 7) = ($)** _____

New Cost: **Baseline Manufacturing Cost ($) - Cost Impact = ($)** _____ **-($)** _____ **= ($)** _____

***Notes:** **Positive Value = Cost Savings**
Negative Value = Cost Increase

Remarks _____

_____

By: _____

Date: _____

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SECTION 4
CONCEPTUAL DESIGN

4.1 Background

In many organizations manufacturing electronic products, a major weakness of the design process has been, historically, the lack of communication between the design engineer and the production engineer; especially early in program development. The designer is actively engaged in keeping abreast of the "state of the art" in electronic design concepts and the production engineer is maintaining knowledge in the "state of the art" of manufacturing processes, materials, and equipment. The MC/DG provides a mechanism for design and production engineers to work in concert at the conceptual design (CD) stage of product development.

The manufacturing cost data and formats for electronics are presented in two major categories, i.e., for use in the conceptual design (CD) and detail design (DD) phases. The information for designer guidance to lowest cost and for conducting manufacturing cost/performance trade-off studies at the conceptual design (CD) phase, is included in this section. The information for use at the detail design (DD) phase is presented in Section 5.

This conceptual design section contains Cost-Driver Effects (CDE) formats. These formats provide input and, hence, experience, from engineers of both disciplines. The CDE formats that comprise the CD section of the MC/DG are shown in Figure 4-1. The various groups of formats, that follow each selection aid, are highlighted, see Figure 4-2.

4.2 Conceptual Design Parameters and Trade-Off Studies

The initial step for the conceptual designer is to conduct a review of the customer requirements and applicable specifications. The system design parameters derived from this review are then listed on the "Conceptual Trade-Off Study Selection Chart", Table 4-1, under the column entitled "Parameter Value". Trade-off studies must, of necessity, be initiated prior to obtaining all indicated system parameters. A trade-off study is an iterative process. Derived data are put into the "Parameter Value" column as each trade-off study progresses.

Six major trade-off studies are listed in Table 4-1 and are discussed in this section. These CD trade-off studies are:

I. Standard Circuits versus New Technology (Section 4.2.1)

II. One versus Multiple Assemblies (Section 4.2.2)

III. System Partitioning; Identical versus Common (Shared) Functions (Section 4.2.3)

IV. Analog versus Digital System Design (Section 4.2.4)

V. Impact of Built-In Test (Section 4.2.5)

VI. Part Package Type versus Available Space (Section 4.2.6)

These design concerns have a large impact on manufacturing costs of an electronic system. The parameters indicated by a solid black dot, in Table 4-1, are the prime cost drivers within a trade-off study. Therefore, study activity must be continued until all design parameters indicated by a solid black dot are optimized. Design optimization is the process that establishes the best relationship between customer requirements and manufacturing cost.

This section also includes CDE formats for the following categories of relative cost information required by conceptual designers:

(a) Part Selection - Packaging (Section 4.2.7)

(b) Part Selection - Reliability (Section 4.2.8).

CONCEPTUAL DESIGN (CD)
FORMAT SELECTION AID

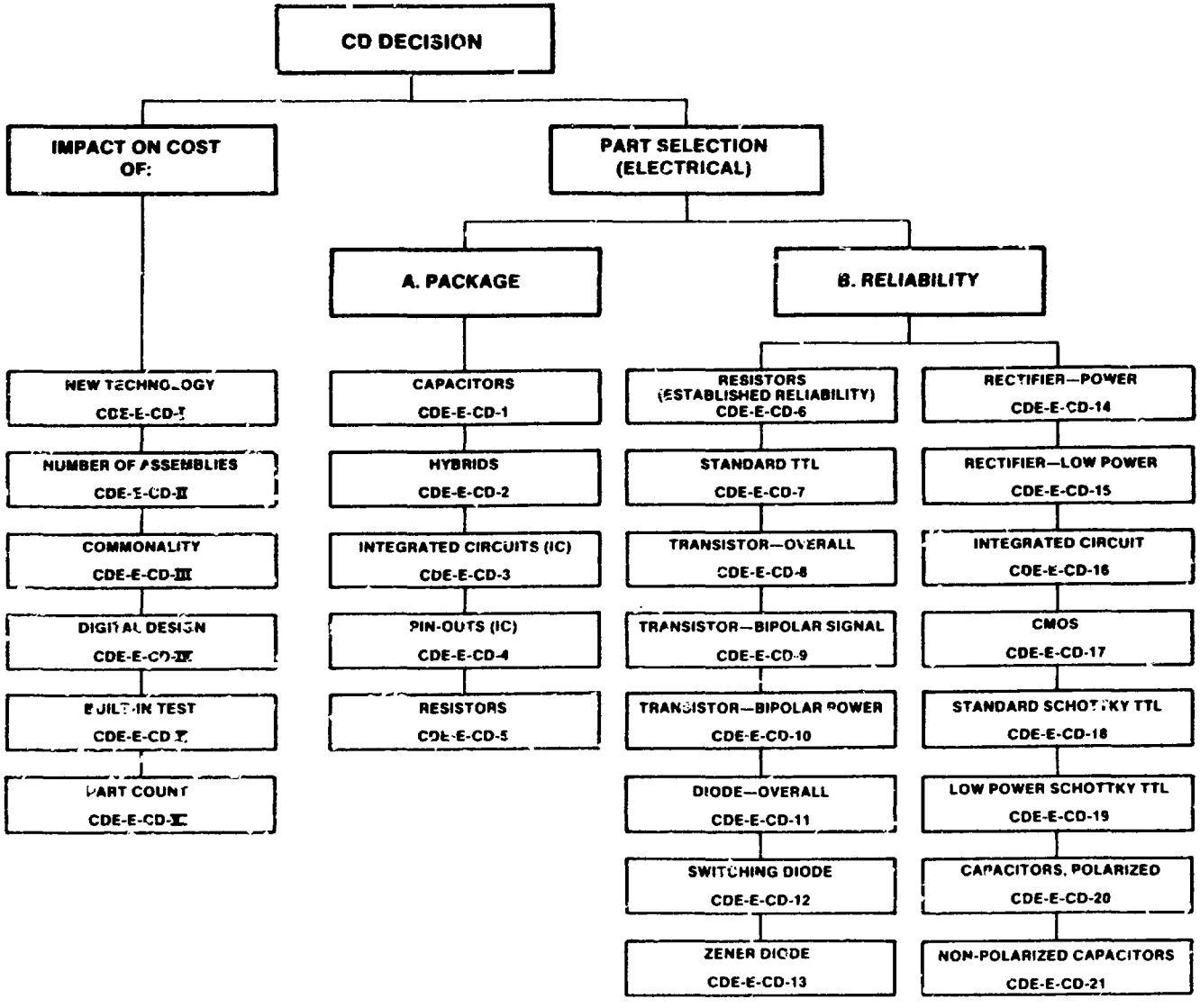

FIGURE 4-1. OVERVIEW SELECTION AID FOR CONCEPTUAL DESIGN

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CONCEPTUAL DESIGN (CD)
FORMAT SELECTION AID

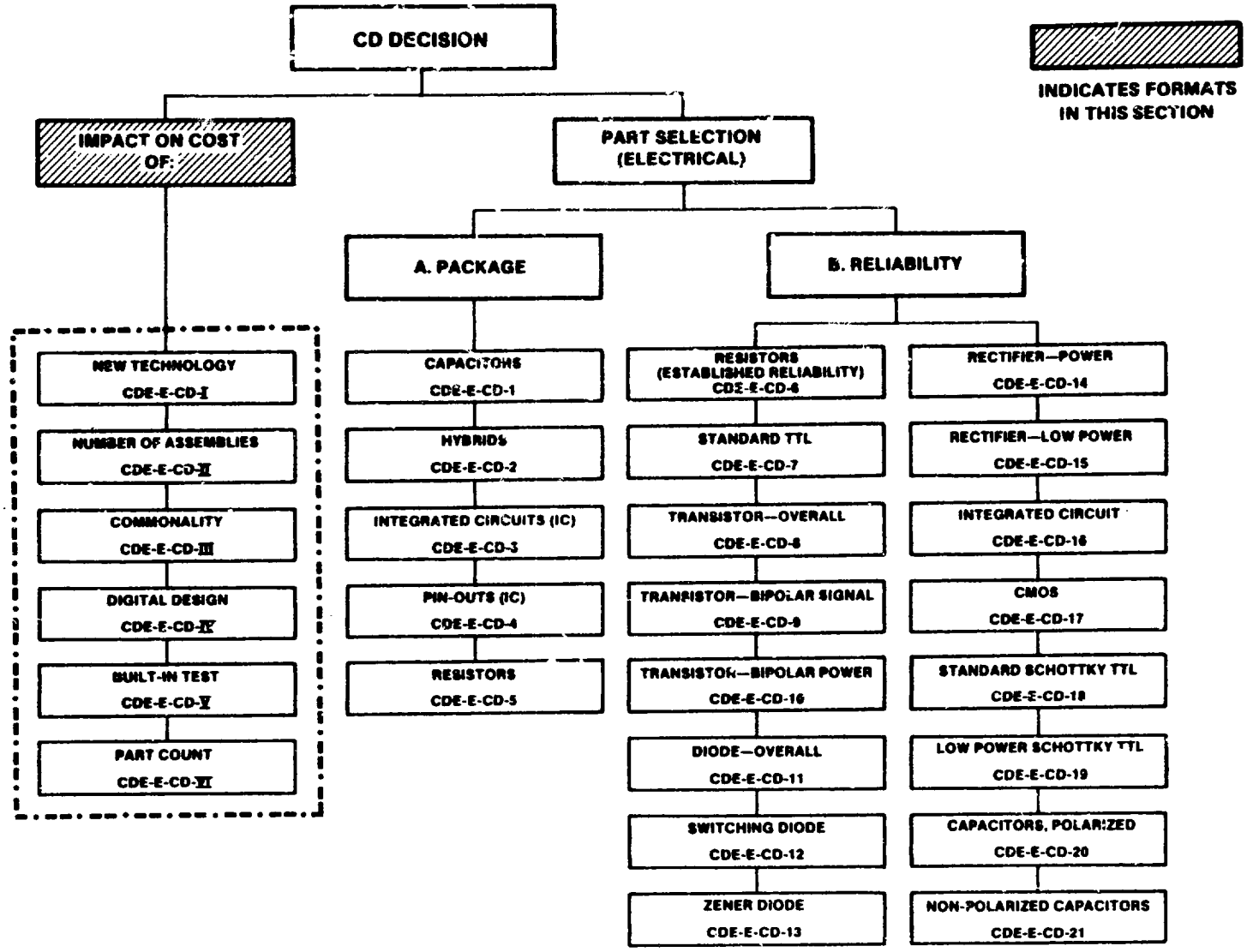


FIGURE 4-2. CONCEPTUAL DESIGN FORMAT SELECTION AID

TABLE 4-1.

CONCEPTUAL DESIGN PHASE TRADE-OFFS DESIGN PARAMETERS REQUIRED

System Design Parameters	Parameter Value (Specified or Developed)	Impact of: New Technology I	Number of Assemblies II	Common Functions III	Digital Design IV	Built-In Test V	Part Count VI
1. Reliability		●	●	●	×	●	●
2. Maintainability		●	×	○	×	●	×
3. Environmental		○	●	○	×	○	×
4. Part Costs		○	×	○	×	×	○
5. Test Cost		●	×	×	×	●	●
6. Assembly Cost		●	×	×	×	×	●
7. Factory Special Handling		●	○	○	○	○	●
8. Part Density		●	×	●	×	○	●
9. Number of Functions		○	○	○	●	×	○
10. Partitioning, Functional		×	●	×	●	×	×
11. Interface (With Other System)		×	●	●	●	×	×
12. Redundancy		×	●	×	●	●	×
13. Maintenance Concept		×	●	○	×	●	○
14. Aircraft Configuration		○	●	×	×	●	○
15. Fault isolation		×	×	●	●	●	×
16. Mission Length		○	○	●	○	○	○
17. Vulnerability Levels		○	●	×	×	×	×

Parameters Required for Use of CDE Formats I-VI

● = Required Data
○ = Secondary Data
× = Not Used

Designer: _____
Date: _____

4.2.1 Conceptual Design Study: Standard Circuits versus New Technology

4.2.1.1 Problem Statement

To determine the impact of a new technology against a baseline configuration mechanized by a design using "standard" or present technology circuits. The trade-off study may be performed at any indenture level of the system. However, to generate data at the assembly of SRU level is less complicated. The format for this trade-off study is CDE-E-CD-I.

4.2.1.2 General Procedure

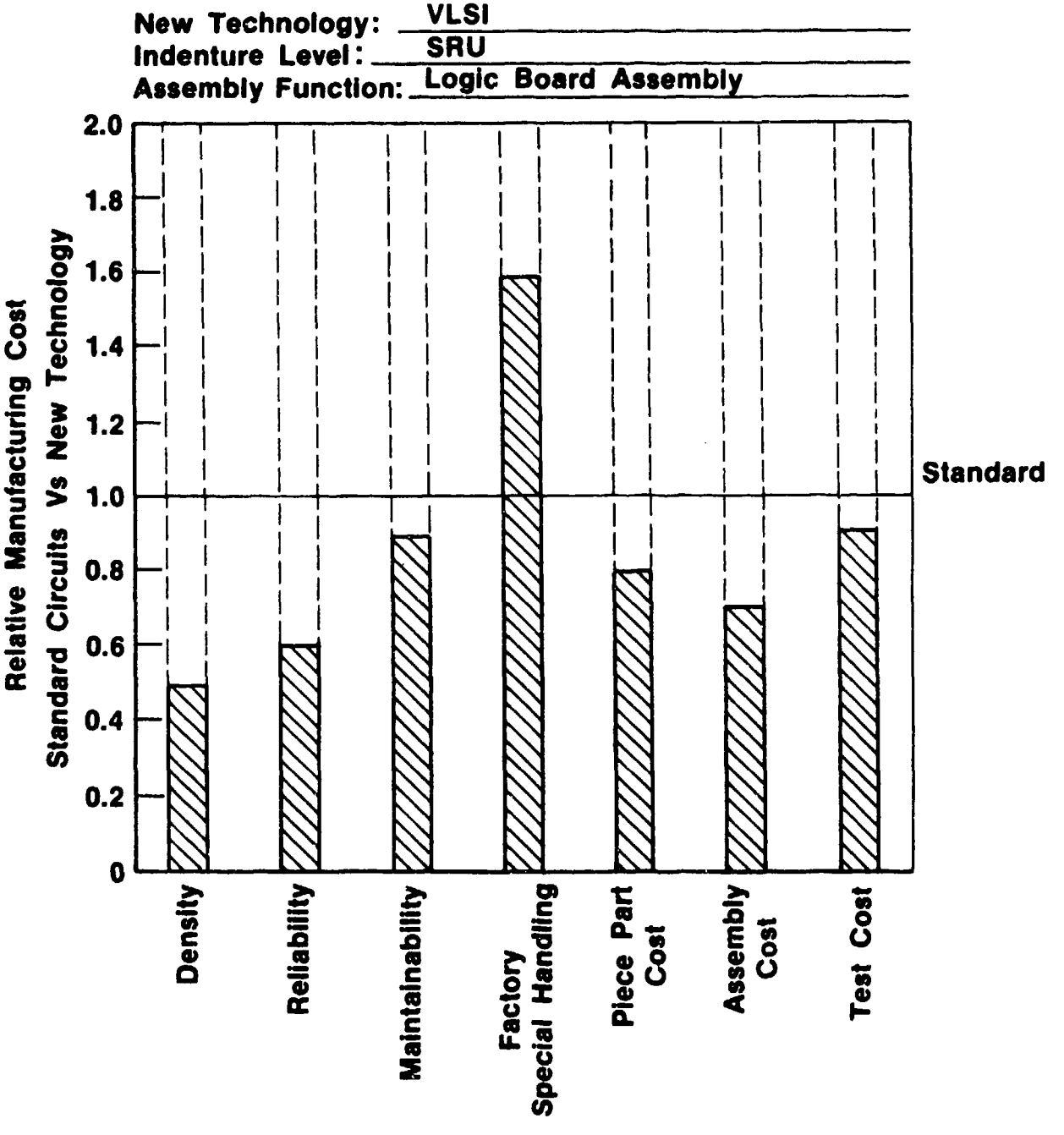
Manufacturing cost is impacted by the seven basic design parameters, Figure 4-3 (CDE-E-CD-I) and Table 4-2, which are analyzed in this study. The trade-off study is accomplished using the following steps:

1. Establish a circuit definition using present day technology.
2. Normalize the seven design parameters to 1.0 for the standard or baseline configuration.
3. Establish a configuration to perform the system requirements by using a new technology.
4. Have design engineering define values for the seven parameters as applied to the new technology and enter the data into Figure 4-3 (CDE-E-CD-I).
5. Using the data of Step 4, apply the "K" factors of Table 4-2 to obtain a weighted contribution of each parameter to the assembly manufacturing cost.
   Note: A negative variance from the baseline indicates higher manufacturing costs.
6. Add the weighted value of all seven parameters. This total provides a relative manufacturing cost of producing the new technology design with respect to the present standard circuit configuration.

The following example uses Figure 4-3 (CDE-E-CD-I) to perform a trade-off study of standard circuits versus a new technology. The example develops a final manufacturing cost relationship for evaluation of a conceptual design in an electronics system for the impact of Very Large-Scale Integration (VLSI) design. The following ground rules are used:

1. New Technology: VLSI
2. Indenture Level: SRU
3. Standard Circuit: Logic board

EXAMPLE TRADE-OFF STUDY
IMPACT OF NEW TECHNOLOGY



CDE-E-CD-I

FIGURE 4-3. CD FORMAT FOR NEW TECHNOLOGY

TABLE 4-2. IMPACT OF NEW TECHNOLOGY
(CDE-E-CD-I)

"K" Factors: Manufacturing Cost Weighting Factors for Design Parameters Evaluated in Trade-Off Study

Design Parameter	"K" Factor
Part Cost	5.0
Assembly Cost	1.5
Test Cost	1.0
Factory Special Handling	1.0
Density	0.5
Maintainability	0.5
Reliability	0.5
	10.0

Note: These "K" factors are defined as general SRU factors for printed circuit assemblies used in military avionic equipment.

4. New technology will be two chips on a card with printed circuit (PC) paths and chassis connector.

5. Factory special handling refers to CMOS grounding requirements. Special handling due to component size or cost, bond room requirements for 100 percent source inspection, etc.

6. Maintainability and reliability factors are considered for the impacts on manufacturing costs due to added piece part test criteria, part level selection, ease of repair for factory test failure, and probability of failures during Manufacturing Run In (MRI) or Acceptance Test Procedure (ATP).

4.2.1.3 Procedure

For this example, the following procedure is used:

1. Establish Baseline: Standard circuits as defined by parts list and assembly costs.

2. Define Trade-Off Study (New Technology): Replace circuit functions of the baseline with two VLSIC's. One Programmable Read-Only Memory (PROM) on a special Integrated Circuit (IC). Equivalent trade-off of standard circuit versus VLSI at the SRU level.

3. Design engineering prepares Figure 4-3 (CDE-E-CD-I) for this trade-off.

4. Apply "K" factors in Table 4-2 (CDE-E-CD-I); the summation of the weighted cost factors provide the values in Table 4-3.

TABLE 4-3
SAMPLE TABLE PROVIDING TRADE-OFF STUDY RESULTS

Design Parameter	Calculation	Weighted Cost Factor
Density	(1.0 - 0.5)K = +0.5 x 0.5 =	+0.25
Reliability	(1.0 - 0.6)K = +0.4 x 0.5 =	+0.20
Maintainability	(1.0 - 0.9)K = +0.1 x 0.5 =	+0.05
Factory Special Handling	(1.0 - 1.6)K = -0.6 x 1.0 =	-0.60
Part Cost	(1.0 - 0.8)K = +0.2 x 5.0 =	+1.0
Assembly Cost	(1.0 - 0.7)K = +0.3 x 1.5 =	+0.45
Test Cost	(1.0 - 0.9)K = +0.1 x 1.0 =	+0.1
		+1.45

The weighted cost factor of 1.45 indicates that the cost of utilizing new technology, with standard technology as the baseline, will be reduced by 55 percent. The advanced technology configuration will result in a net savings in manufacturing costs.

4.2.2 Conceptual Design Study: One Assembly versus Multiple Assemblies

4.2.2.1 Problem Statement

To determine the manufacturing cost impact of producing one assembly or building multiple assemblies to package an avionics system in an aerospace vehicle. For this conceptual study, the line replaceable unit (LRU) indenture is the intended study level. Some systems may lend themselves to a subassembly study, if the subassembly is a distinct package with a specific system function, i.e., a pressure transducer assembly mounted in an LRU. The format for this trade-off study is CDE-E-CD-II.

4.2.2.2 Procedure

For this trade-off study, nine system design parameters, Figure 4-4 (CDE-E-CD-II) are rated by cost-evaluation ratios for up to four identical assemblies. Relative manufacturing costs are then determined for each system configuration with no approach considered as baseline for a normalized evaluation. It is necessary that the design and production engineers approach this study from the viewpoint of the system configuration.

The cost-weight factors are arrived at for a given system by starting with a basic four-channel redundant avionics function. The cost-weight factor for each design parameter must be generated for each system studied inputting the derived data on Figure 4-4 (CDE-E-CD-II). The obvious packaging concept may seem to be manufacturing four identical boxes with four identical function selectors or control panels to enable redundance levels to be maintained with the outside world interfaces.

The following sample trade-off study reviews the four-box system with regard to various levels of control panel redundancy.

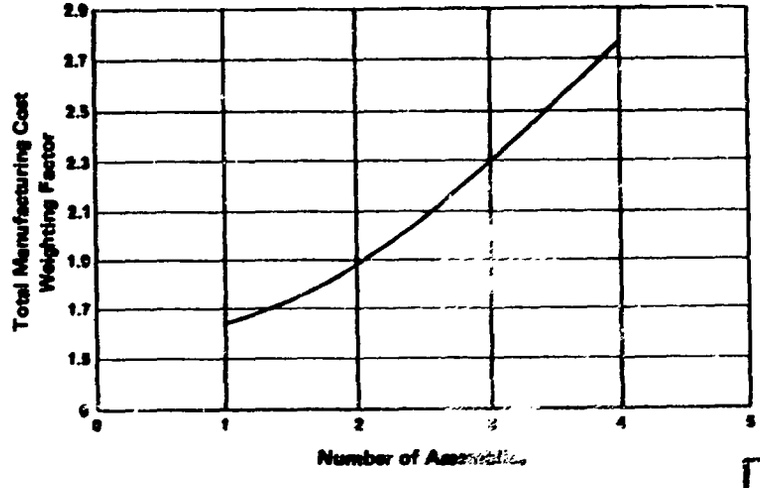
Block diagrams of the example of this trade-off study are shown in Figure 4-5 (CDE-E-CD-IIA). Two major changes occur with each concept change. First, the cabling between the control panel(s) and the system becomes considerably less complex when the number of panels is reduced. Cross channel monitoring and logic control lines become easier to handle as the interface box or control panel redundancy is reduced. Second, the configuration or design of the control panel becomes more complex as the number of panels is reduced. Each switch must have more panels and contacts. Logic status must be displayed differently and system faults require more logic circuits to interpret and display status data. The lower redundancy levels of the control panel greatly impact the system mission reliability and must be factored into the manufacturing cost trades.

Figure 4-4 (CDE-E-CD-II) depicts the cost weight factors for the system design parameters as defined for the sample trade-off study for

SAMPLE FORMAT CDE-E-II

EXAMPLE TRADE-OFF STUDY

System Design Parameters	Cost Weight Factor: One Assembly	Two Assembly	Three Assemblies	Four Assemblies
Vehicle Configuration	0.05	0.1	0.2	0.5
Redundancy Level	0.0	0.2	0.4	0.5
Vulnerability Level	0.5	0.3	0.1	0.05
Identical Configuration	0.0	0.1	0.2	0.3
Maintenancy Philosophy	0.0	0.1	0.2	0.3
System Reliability	0.5	0.4	0.3	0.1
Interconnects	0.0	0.1	0.2	0.3
Environmental Impacts	0.1	0.2	0.4	0.6
Functional Partitioning	0.5	0.4	0.3	0.1
Total Cost Weighting Factor	1.65	1.90	2.30	2.75



CDE-E-CD-II

FIGURE 4-4. TRADE-OFF STUDY: SINGLE VS. MULTIPLE ASSEMBLIES

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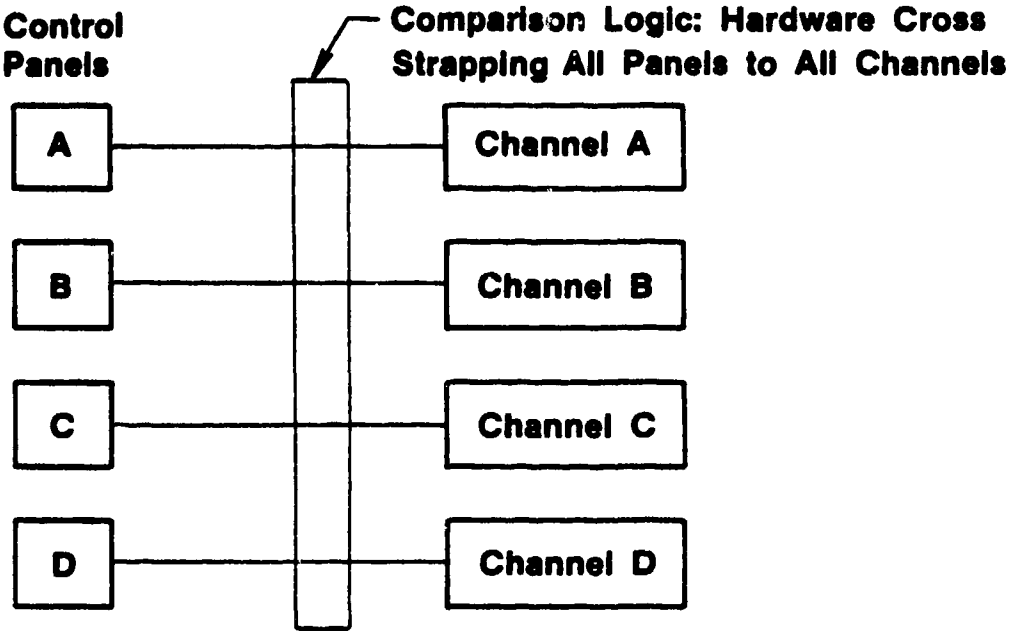
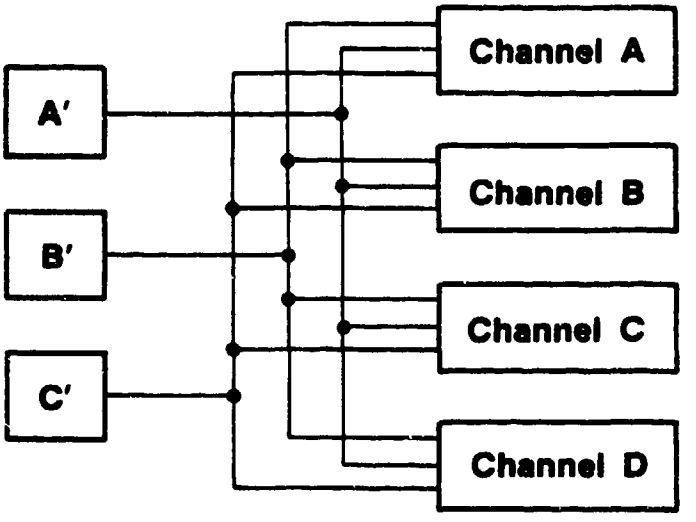
MULTIPLE ASSEMBLY TRADE-OFF STUDY

Concept A: 4 Channels, 4 Control Panels



Concept B: 3 Control Panels

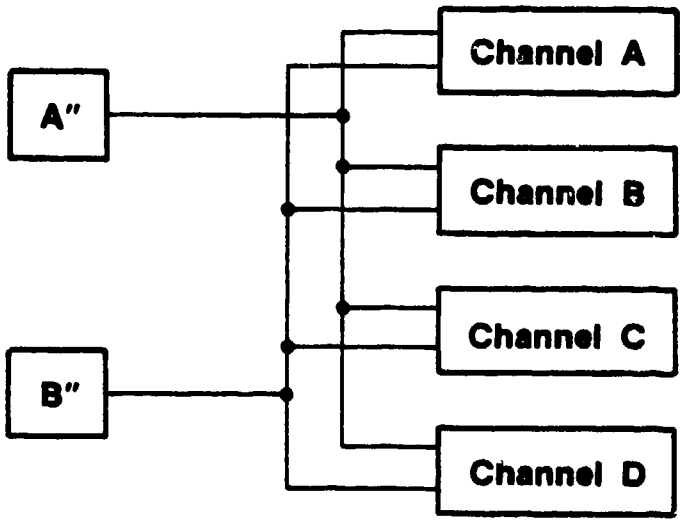


CDE-E-CD-IIA

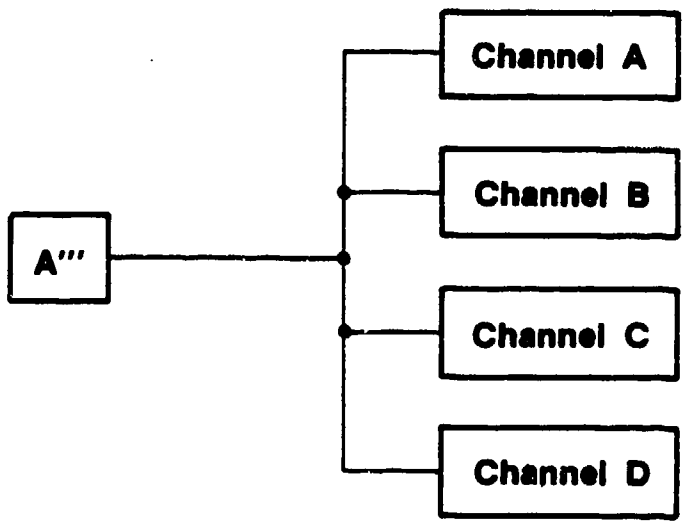
FIGURE 4-5. MULTIPLE ASSEMBLY TRADE-OFF STUDY

MULTIPLE ASSEMBLY TRADE-OFF STUDY (Continued)

Concept C: 2 Control Panels



Concept D: 1 Control Panel



(Continued)

CDE-E-CD-IIA

FIGURE 4-5. MULTIPLE ASSEMBLY TRADE-OFF STUDY (Continued)

the number of control panels for a four-channel system. The cost-weight factors for each design parameter must be generated for each system studied.

The curve plotted as part of Figure 4-4 (CDE-E-CD-II) graphically depicts the relative manufacturing costs for each concept.

4.2.3 Conceptual Design Study: System Partitioning; Identical versus Common Functions

4.2.3.1 Problem Statement

The conceptual design phase of a program may indicate several alternative partitioning approaches to a system configuration which will enable the use of commonality concept or time-shared functions (Figure 4-6). The manufacturing cost may be significantly impacted by the design approach. This trade-off study enables the system design engineer to weigh the manufacturing cost impacts early in product development. The format for this trade-off study is CDE-E-CD-III.

4.2.3.2 Procedure

Six system design parameters (Table 4-4), have been selected for evaluation, as the significant manufacturing cost drivers, in this trade-off study example. These parameters are:

1. Shared Assembly - Increased complexity of the one assembly.
2. Reliability - The impact of system reliability for each partitioning approach.
3. Density - The impact of piece part density on common/unique assembly designs.
4. Interconnects - Complexity of cross channel coupling or monitoring and build and test cost impacts.
5. Fault Isolation Capability - Complexity of BIT configuration or continuous fault monitoring circuitry.
6. Mission Length - Longer operating time impact on mission success probability.

Past experience has generally been accumulated with designs using identical circuits when partitioning a system. The available data on these systems are normalized to evaluate relative costs for the design parameters under study.

The system evaluated for this example is an existing avionics system consisting of three independent, redundant channels of electronics. Each channel has identical circuits and contains its own central processing unit or CPU. The shared function is mechanized with the same three electronics channels; however, the channel outputs are controlled by one CPU (Figure 4-6).

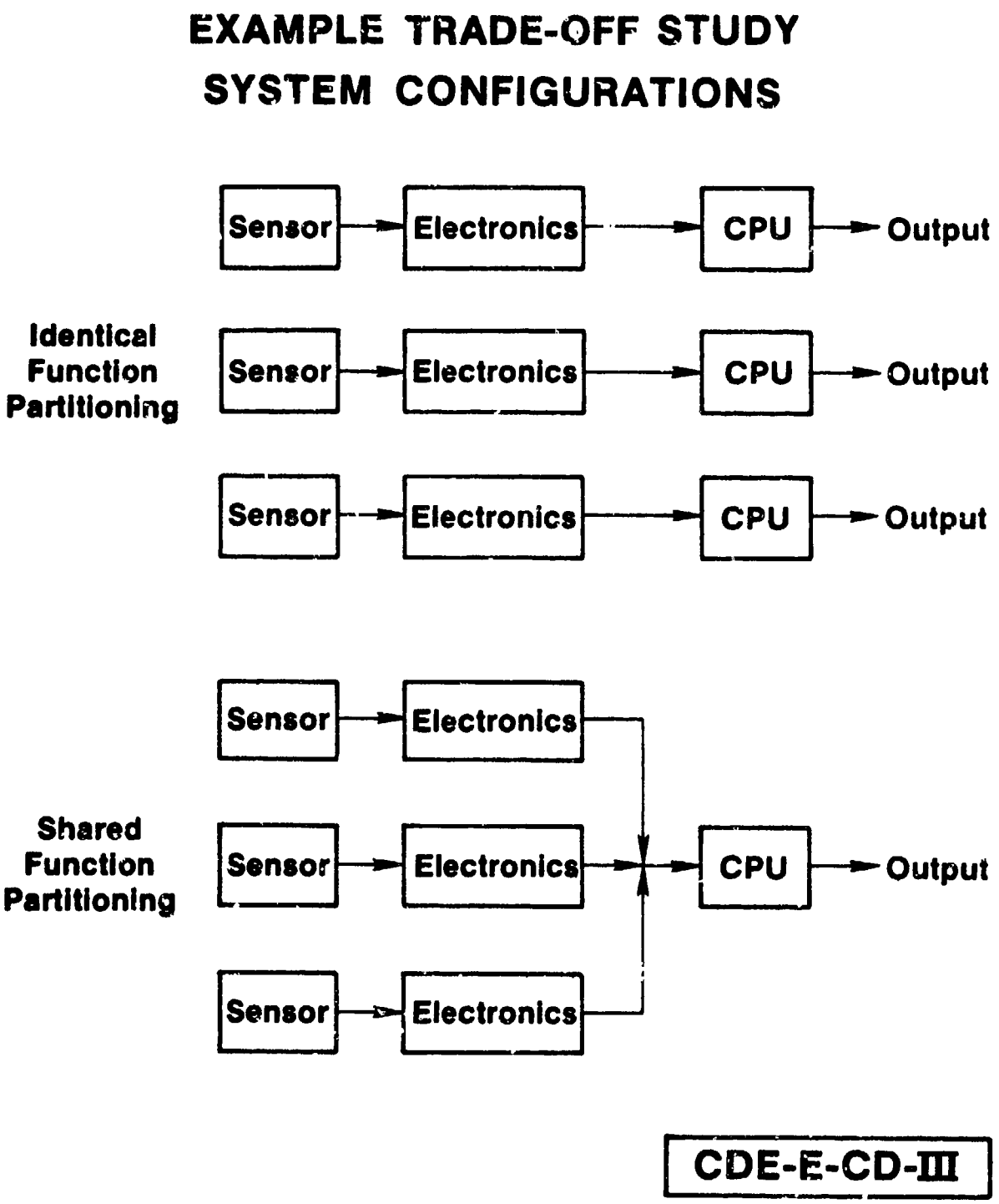


FIGURE 4-6. EXAMPLE OF SYSTEM CONFIGURATIONS

The procedure for performing this trade-off study of identical functions versus shared functions requires the designer to generate data for the above six design parameters in developing the format of Figure 4-7 (CDE-E-CD-IIIA). The parameters are normalized to 1.0 for the baseline configuration.

Table 4-4 (CDE-E-CD-III) has "K" factors for weighing the design parameters developed in the format. The procedure and results are shown in Table 4-5.

Figure 4-8 (CDE-E-CD-IIIB) shows the design parameters of the shared function configuration with respect to the normalized identical configuration. This figure applies the "K" factors to obtain a weighted contribution of each design parameter to the system manufacturing cost.

The results of this trade-off study indicate that the shared function partitioning is more costly than partitioning with identical circuits. The data indicate the necessity of iterative studies to weigh all configurations with respect to manufacturing costs.

EXAMPLE TRADE-OFF STUDY (Continued)
IMPACT OF COMMONALITY

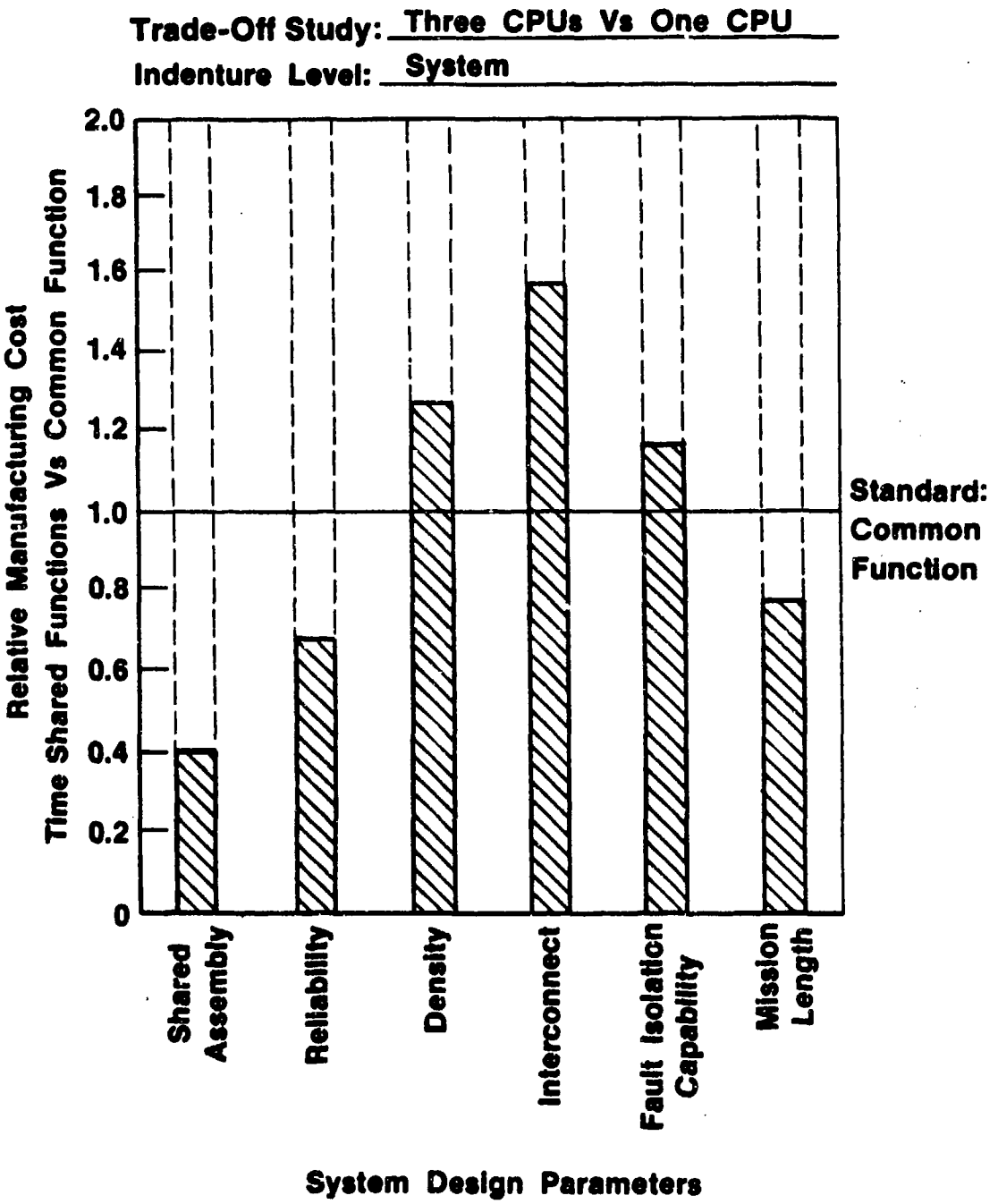


FIGURE 4-7. CD FORMAT FOR COMMON FUNCTIONS

IMPACT OF COMMONALITY

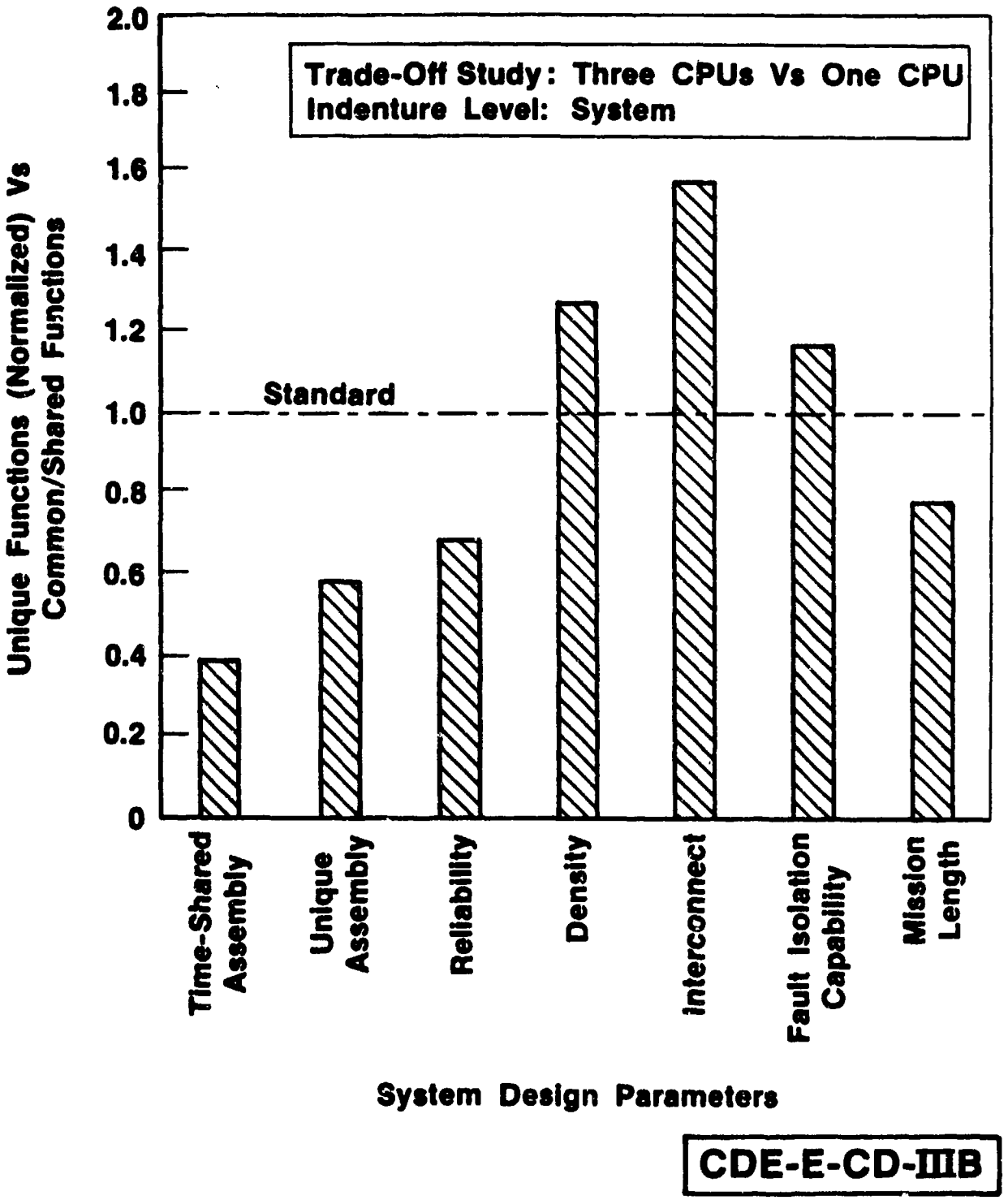


FIGURE 4-8. CD FORMAT FOR COMMON FUNCTIONS
(Continued)

TABLE 4-4. IMPACT OF COMMONALITY
(CDE-E-CD-III)

"K" Factors: Manufacturing cost-weighting factors for design parameters evaluated in trade-off study.

Design Parameter	"K" Factor
Shared Assembly:	2.5
Reliability:	2.0
Density:	2.0
Interconnects:	1.0
Fault Isolation Capability:	1.5
Mission Length:	1.0
	10.0

TABLE 4-5. SAMPLE TRADE-OFF STUDY RESULTS

Design Parameter	Calculation	Weighted Cost Factor
Shared Assembly:	(1.0 - 0.4) K = +0.6 x 2.5 =	+1.5
Reliability:	(1.0 - 0.4) K = +0.6 x 2.0 =	+1.2
Density Impact:	(1.0 - 1.3) K = -0.3 x 2.0 =	-0.6
Interconnects:	(1.0 - 1.6) K = -0.6 x 1.0 =	-0.6
Fault Isolation Capability:	(1.0 - 1.4) K = -0.4 x 1.5 =	-0.6
Mission Length:	(1.0 - 0.8) K = +0.2 x 1.0 =	+0.2
		1.1

4.2.4 Conceptual Design Study: Analog versus Digital System Design

4.2.4.1 Problem Statement

To define the basic configuration as to a digital system or an analog system design. At the start of the conceptual design phase, an early decision is often required to define the functions required to meet operational specifications. The most immediate task is to define an interface list to provide signal types, signal levels, termination impedances, dedicated or time shared data transmission, and power requirements. The format for this trade-off study is CDE-E-CD-IV.

4.2.4.2 Procedure

The curves in Figure 4-9 (CDE-E-CD-IVA) were developed from data obtained by analyzing seven systems. All systems were avionic flight hardware. In two cases, an original analog system was replaced by a digital system performing identical functions. The normalized manufacturing costs as a function of part count are plotted. This curve is not totally usable since piece-part count alone does not account for the capacity of digital processing equipment to accomodate more functions than analog circuits.

The "K" factor curve of Figure 4-10 (CDE-E-CD-IVB) was derived by analysis of the various analog and digital systems to define a relationship of piece-part count to functional capability.

The final results of the analysis are presented in Figure 4-11 (CDE-E-CD-IVC). From this format, a design engineer can determine relative manufacturing costs of an analog versus a digital system mechanization by making a piece-part count and locating the point on the appropriate line of Figure 4-11.

Using the adjusted piece-part count criteria of a summation of all types of electronic parts, the breakpoint for manufacturing cost consideration is 2,100 piece parts.

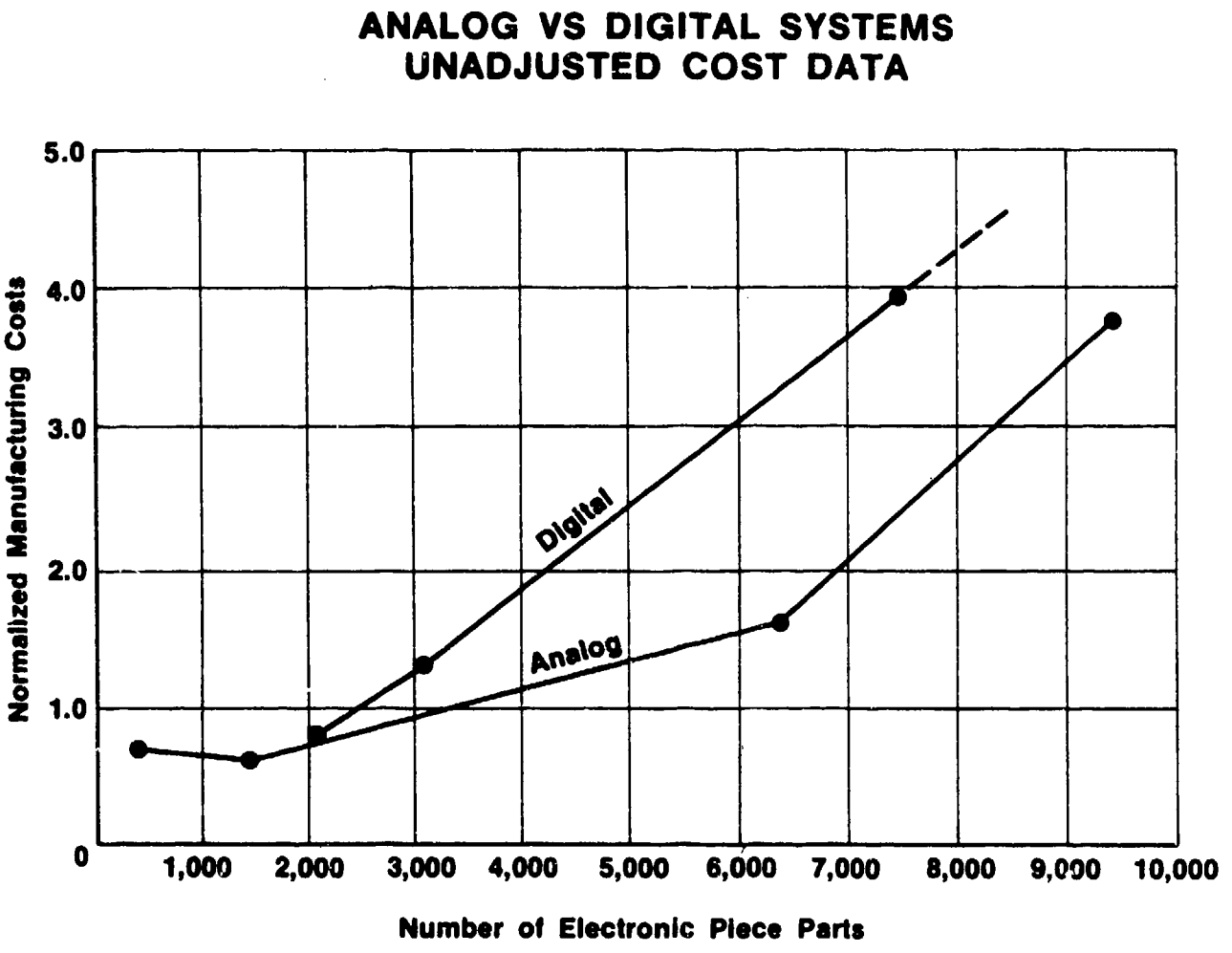
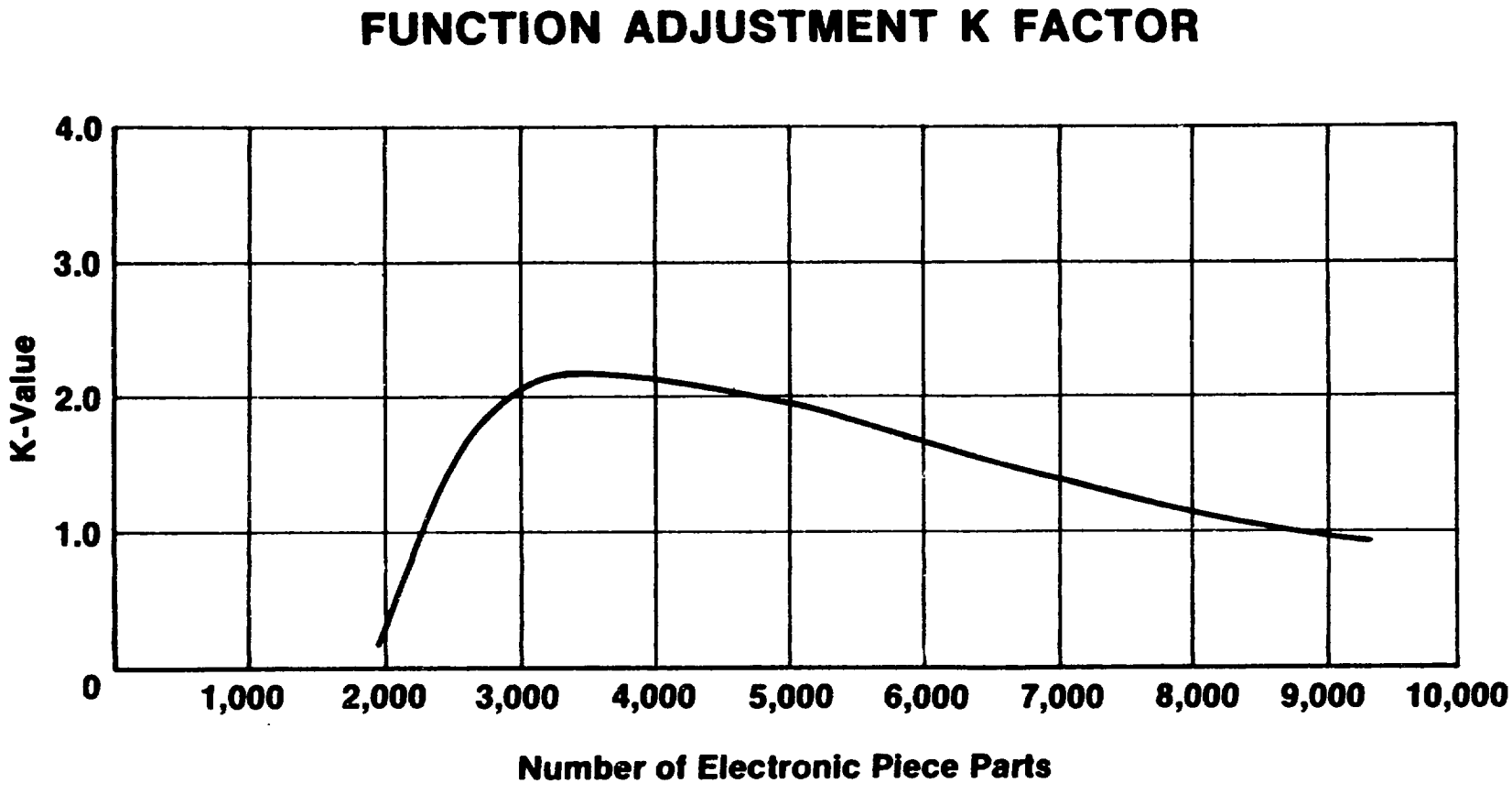


FIGURE 4-9. UNADJUSTED PART COUNT COST DATA FOR ANALOG AND DIGITAL SYSTEMS



CDE-E-CD-IVB

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3 Jan 1983

FIGURE 4-10. FUNCTION ADJUSTMENT FACTOR FOR PIECE-PART COUNT

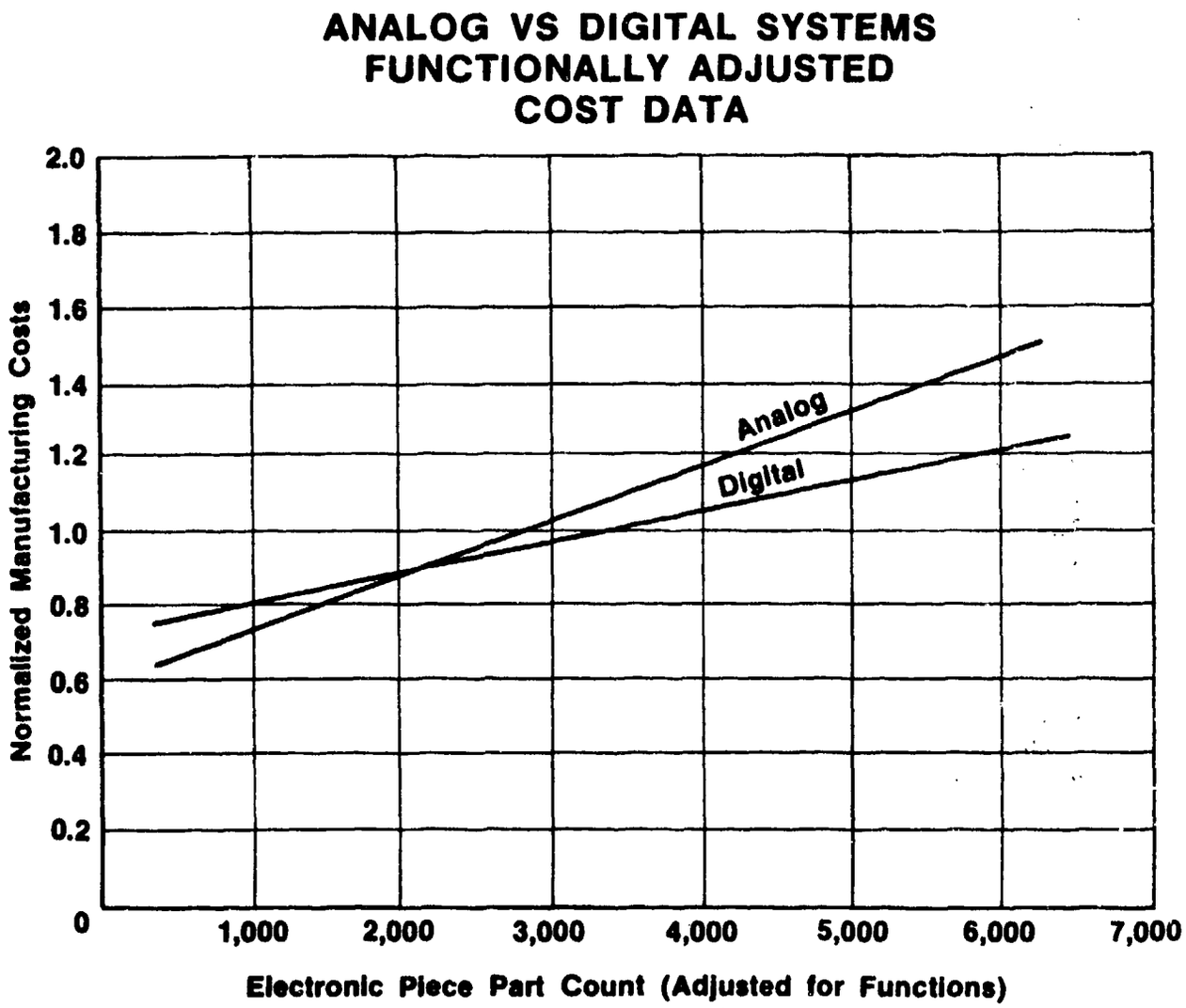


FIGURE 4-11. MANUFACTURING COST FOR FUNCTIONALLY ADJUSTED ANALOG AND DIGITAL SYSTEMS

4.2.5 Conceptual Design Study: Impact of Built-In Test

4.2.5.1 Problem Statement

The objective of this study was to determine whether or not the MC/DG methodologies are applicable to the complex concern of built-in test (BIT). BIT encompasses performing:

- Engineering tests
- Qualification tests
- Burn-in tests
- Fault Isolation to Line Replaceable Unit (LRU)
- Fault Isolation to Shop Replaceable Unit (SRU)
- Maintenance tests.

To determine the impact of BIT on manufacturing cost in this conceptual design study, a segment of the many BIT interfaces has been selected. The conceptual design format for this trade-off study is shown in Figure 4-14 (CDE-E-CD-V).

4.2.5.2 Procedure

The interaction of line replaceable unit, built-in test, manufacturing test, and related equipment has the potential of providing a reduction in manufacturing costs. Four possible benefits of this interaction are:

- Simple ATE to item interfaces - many interfaces that would have to be brought out of the LRU to the ATE are now examined by the BIT.
- Less ATE execution time - more testing is done by the BIT resulting in reduced ATE memory and test time. Also less test software needs to be generated.
- Improved intermittent fault detection - BIT, operating continuously, has a far greater possibility of detecting an intermittent fault, recording that fault, and storing it in a fault memory for later interrogation by the ATE.
- A more comprehensive test - the BIT, being an intimate part of the LRU, is responsive to faults the ATE could not detect due to the limits of interfacing and non real-time monitoring.

In general, the following discussion is directed toward the 15 to 25 board system. Cost impacts vary with system complexity and the required BIT. However, this level of complexity is typical and offers some up-to-date data. The self-test must be capable of annunciating faults it detects such that an operator may isolate the problem to a

card or group of cards and/or function. Also assumed is a relatively thorough level of electronic card test such that an operator, on having a fault annunciated, can remove the suspect assembly or assemblies and subject them to a more detailed test.

Prior to examining the cost differentials associated with BIT/manufacturing test interaction, some definitions of the system configurations involved must be discussed. Figure 4-12 (CDE-E-CD-VA) shows a two-board "system" with two separable functions occupying Board No. 1 and two functions on Board No. 2. Board No. 2 is also broken into subfunctions which are designated "clusters" of components. Clusters are difficult to define, but would consist of subfunctions within a major function, each having a measurable interface.

An end-to-end test is relatively simple, requiring a minimum of test equipment, and isolating nothing except the system. At the opposite end, the test, which isolates clusters of components, requires extensive interfacing equipment diagnostic programming. Board and function isolation fall in between. This relationship is shown in Figure 4-13 (CDE-E-CD-VB), which depicts the relative BIT sizing for the three levels of tests.

The growth in time and part count of roughly 7.5 percent for an end-to-end test reflects the additional memory for the program, as well as the buffering electronics necessary to transfer information to the testing processor. To isolate to a board or function, approximately 27 percent increase in parts is required for an isolation ambiguity of 23 percent between two boards or functions.

To extend the approximation to a detection of faulty clusters of components requires some assumptions. Each function or board type is listed below, and a "cluster breakdown" is provided.

Function	Clusters	Total Clusters	Necessary Tests Added
Processor	ALU, PROM, Logic	3	3
Memory	4 chip address groups	16	0
Analog input	Buffers, A/D	20	1
Analog output	D/A buffers & hold	20	1
Discrete-in	-	10	1
Discrete-out	Each discrete	20	20
Servo amp	Each amplifier	4	4
Resolver input	Each resolver buffer	8	8
Power supply	-	1	6
Demodulator	Each demod	8	8
			52

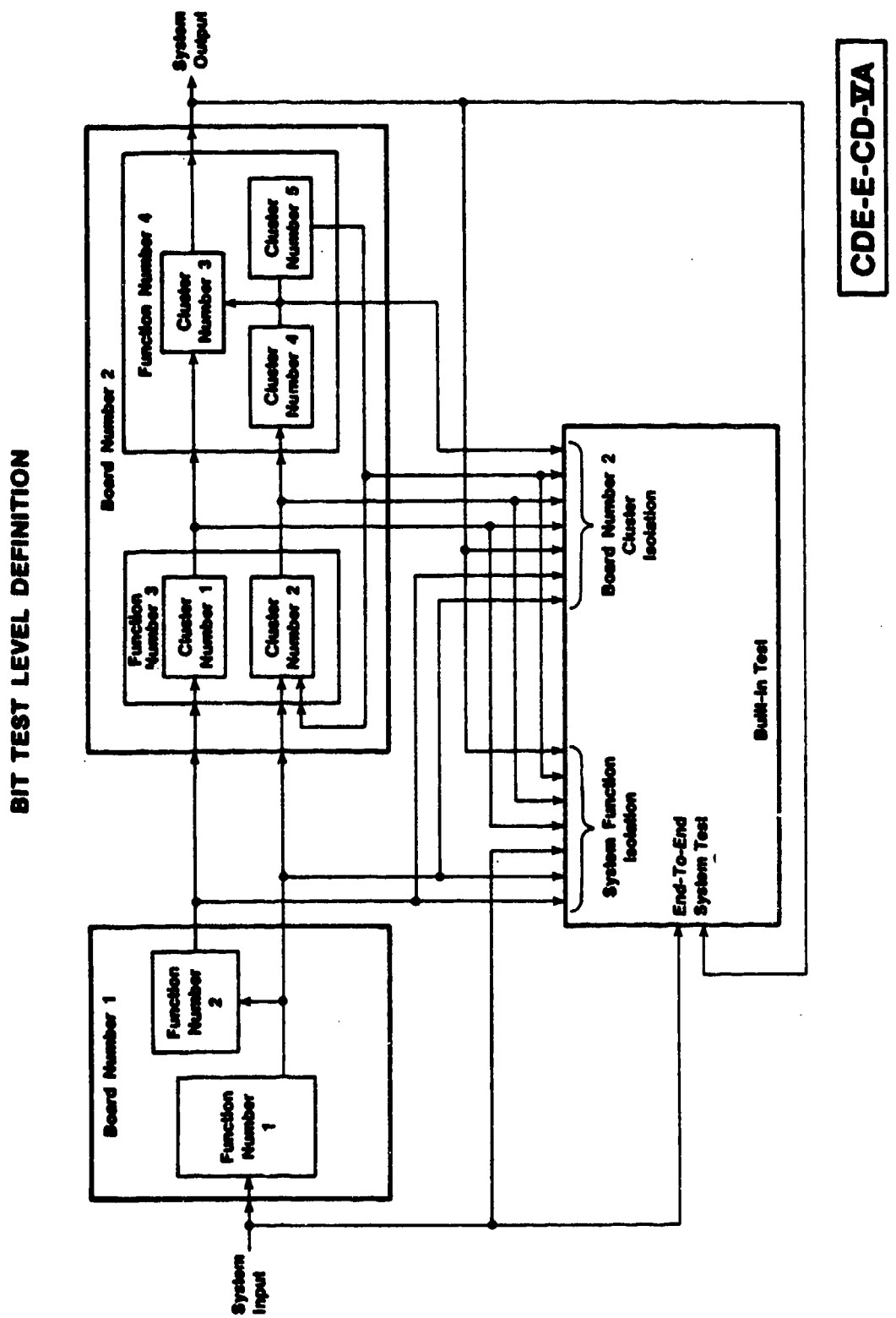


FIGURE 4-12. BUILT-IN TEST LEVEL DEFINITION

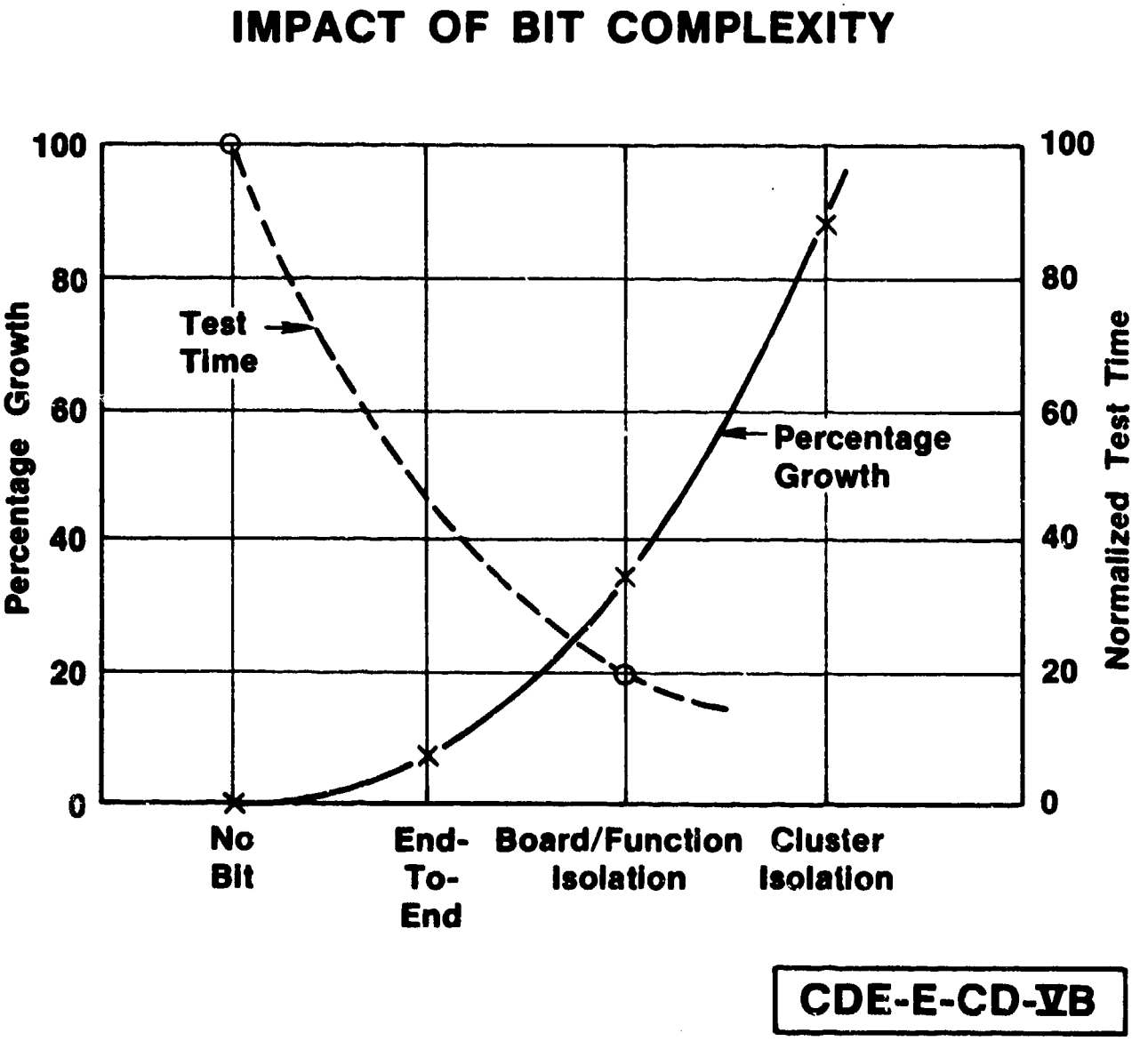


FIGURE 4-13. CD FORMAT FOR BUILT-IN TEST COMPLEXITY

BIT IMPACT ON MANUFACTURING COST

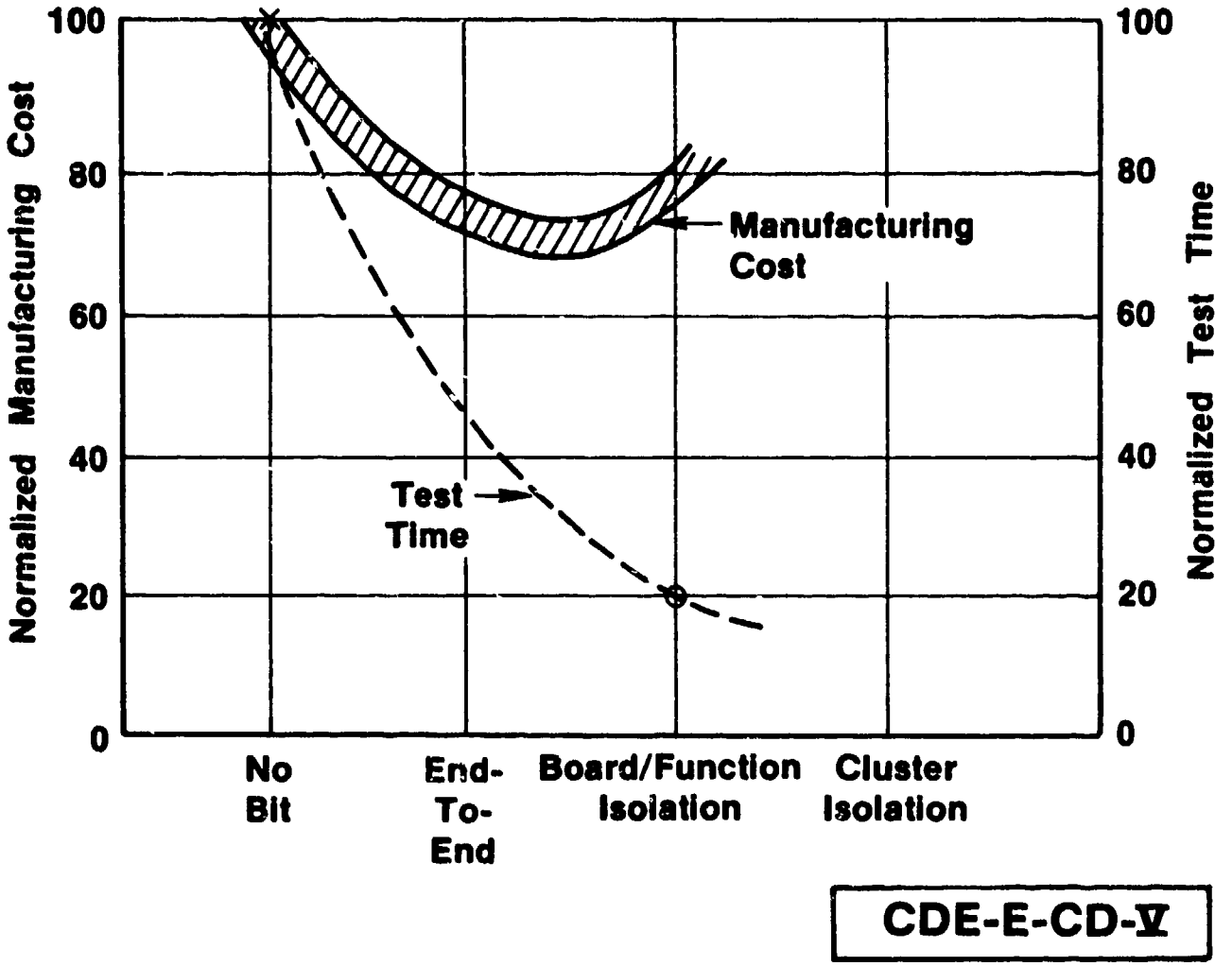


FIGURE 4-14. IMPACT OF BIT ON MANUFACTURING COST

These tabulations provide the basis for the last data point on Figure 4-13 (CDE-E-CL VB).

Once the estimates for the increase in size of the LRU due to BIT are known, an approximation to manufacturing costs can be made. Data indicate that on the average, testing is about 40 percent of the manufacturing cost. This percentage, of course, is a function of board and system complexity, and the type of test equipment involved. The 60 percent balance is composed of parts cost and assembly labor, and is impacted by the level of BIT installed in the LRU. Data also indicate that test time is reduced by a factor of 5 to 12 when a comprehensive, well annunciated BIT is used. Using these figures, the curve of Figure 4-14 (CDE-E-CD-V) was plotted. These are approximations and are useful for indicating trends only. As expected, the test time decreases significantly due to the BIT usage. However, the cost of the increased amount of BIT hardware soon becomes more dominant, and the manufacturing costs begin to rise again, having once reached a minimum. Consequently, it would appear that a relatively thorough BIT may not be cost-effective when considering only manufacturing costs.

4.2.6 Conceptual Design Study: Part Package Type versus Available Space

4.2.6.1 Problem Statement

To determine the relationship of part count to available space using a common denominator to measure against the available board space in an electronics design. The format for this trade-off study is CDE-E-CD-VI.

4.2.6.2 Procedure

The transistor in its various packaging formats is chosen to relate the manufacturing-cost impacts to part count. Two formats are presented to enable the designer to obtain relative manufacturing costs, both material and subsequent assembly, for trade-offs of various design configurations. Figure 4-15 (CDE-E-CD-VIA) relates the number of transistors per square inch of board space to relative manufacturing costs for leadless carrier packaging.

A designer is provided with a card space of 10 $in.^2$ on which a function that requires 1000 transistors to mechanize must be performed. Analysis of the leadless carrier package indicates a choice limited to LSI at 300:1, hybrid at 900:1, and VLSI at 1500:1, where the ratio is with respect to cost per transistor. Analysis of the Dual In-Line Package (DIP) indicates a wider choice with price advantages. DIP is shown in Figure 4-16 (CDE-E-CD-VIB) with VLSI at 1000:1, hybrid at 600:1, LSI at 200:1, MSI at 7:1, and SSI at 5:1, where the ratio is with respect to cost per transistor. Because the required density for the design eliminates the discrete mechanization alternative, the SSI mechanization achieves the lowest manufacturing cost.

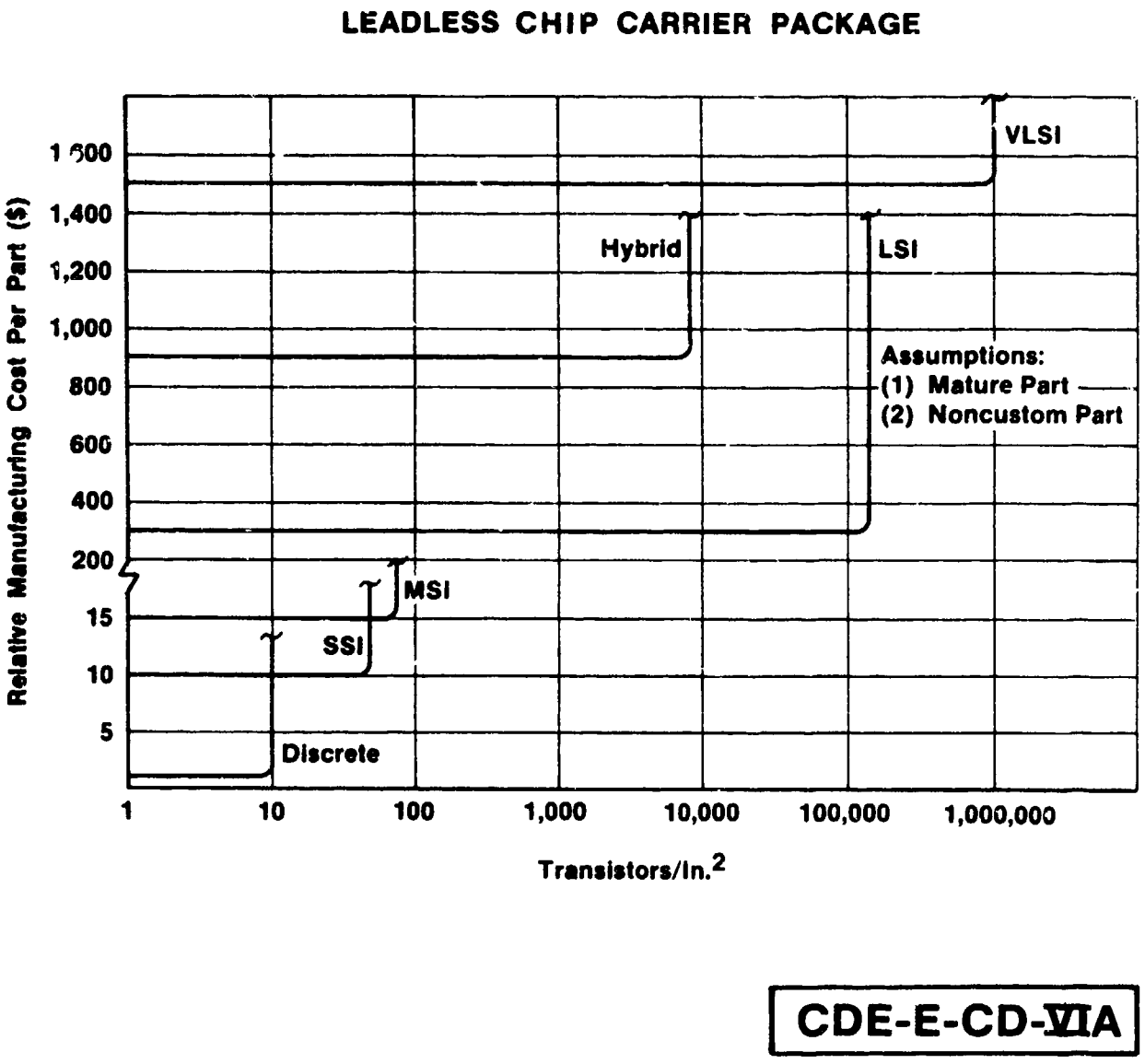
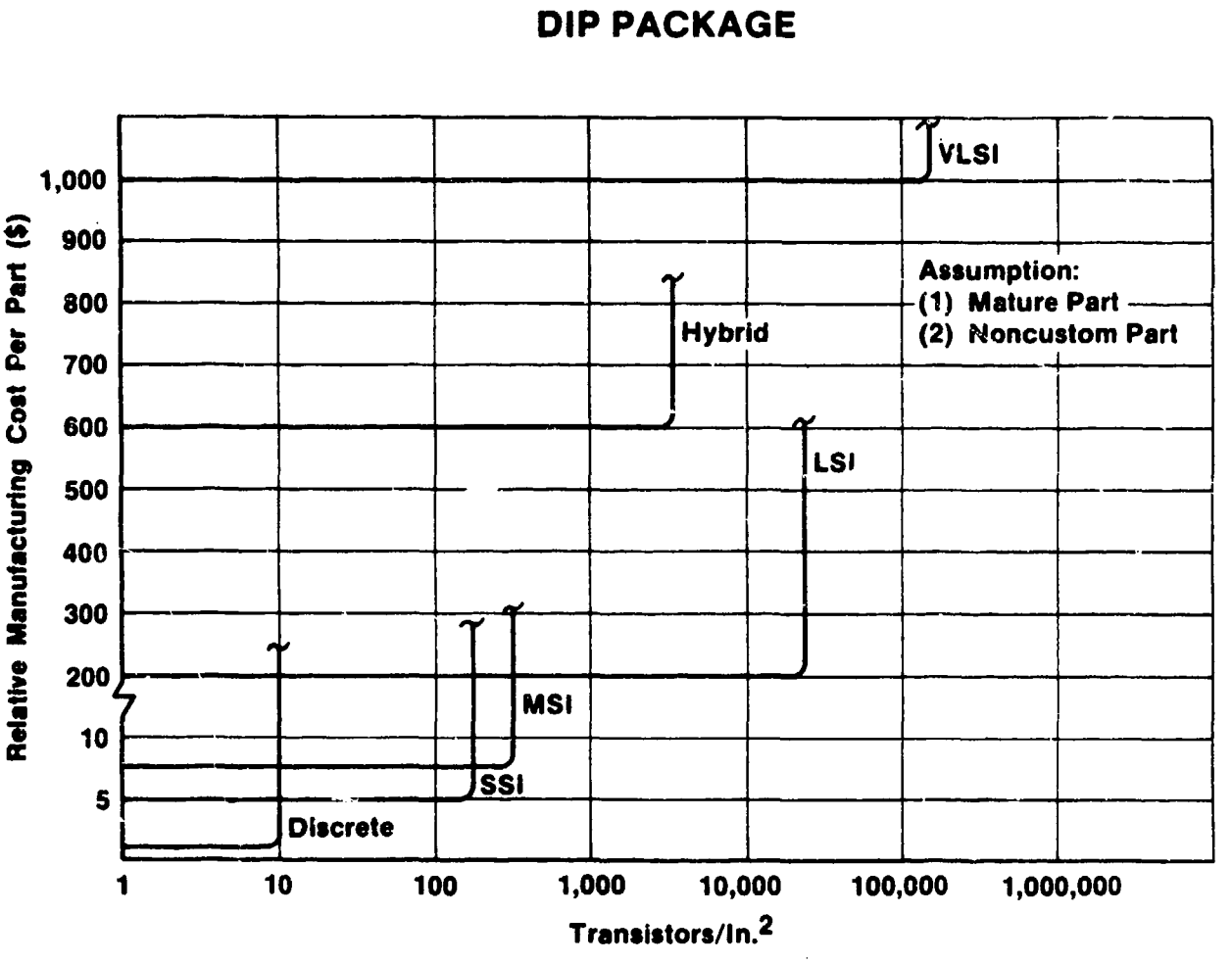


FIGURE 4-15. CD FORMAT FOR MANUFACTURING COST OF LEADLESS CHIP CARRIER PACKAGE



CDE-E-CD-VIB

FIGURE 4-16. CD FORMAT FOR MANUFACTURING COST OF DUAL IN-LINE PACKAGE

4.2.7 Part Selection - Package Section

This section contains the format selection aid and formats for part selection and packaging of electronic assemblies. Example assemblies are integrated circuits and resistors. The formats presented in this section include cost-driver effects (CDE) and cost estimating data (CED).

4.2.7.1 Format Selection Aid

The format selection aid (Figure 4-17) indicates all the formats that can be utilized in the conceptual design process. Those related to packaging are highlighted by the shaded box.

Some formats will be applicable at both the conceptual and detail design phases of electronic systems.

CONCEPTUAL DESIGN (CD)
FORMAT SELECTION AID

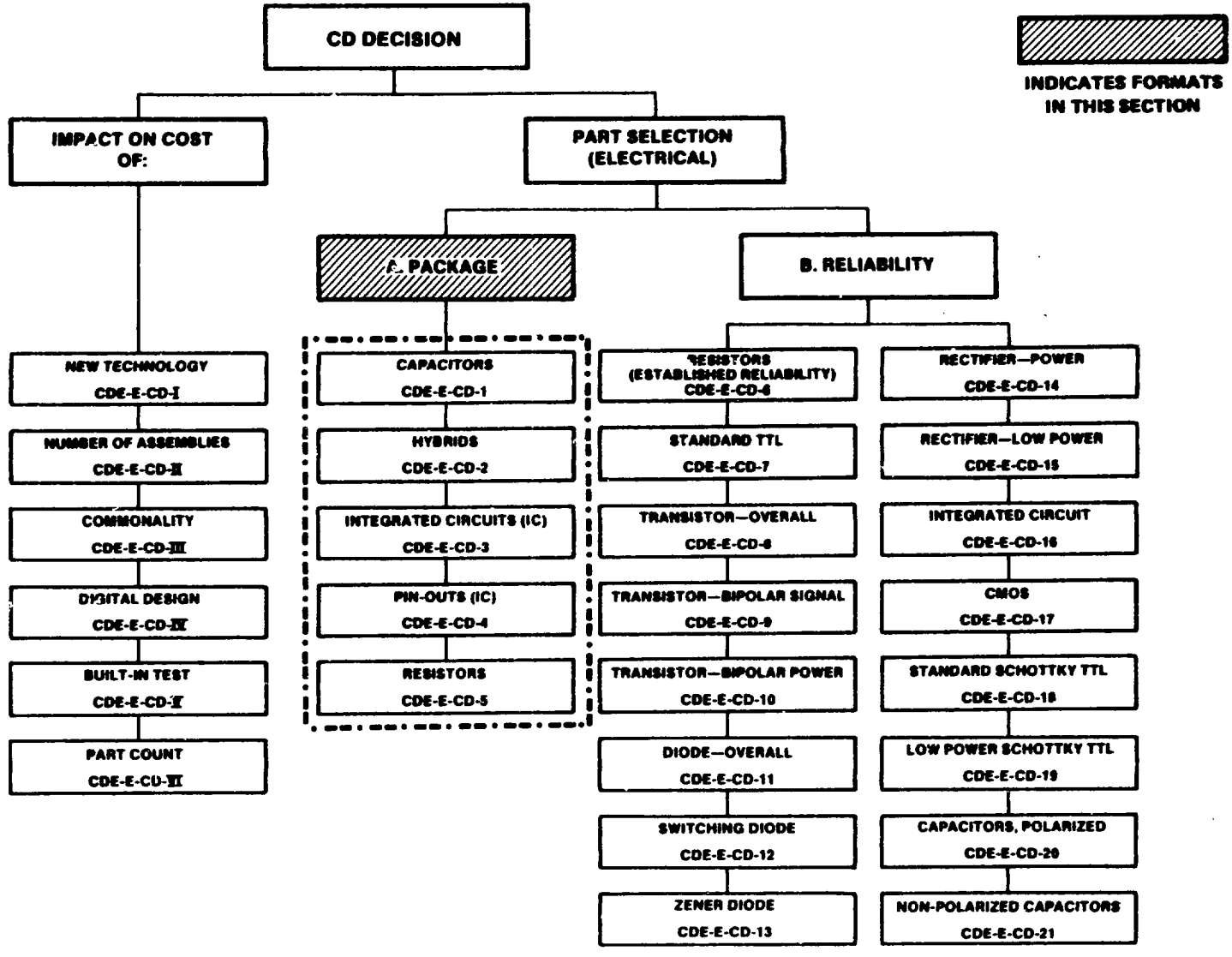
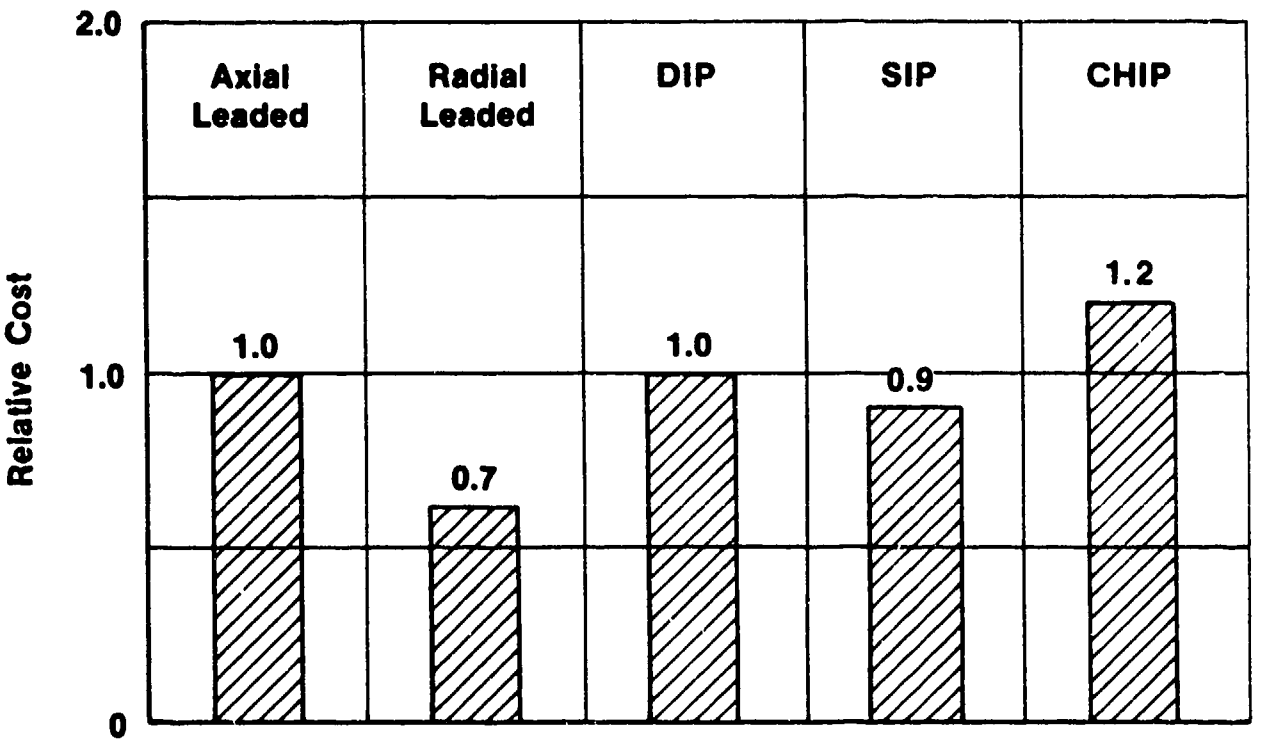


FIGURE 4-17. CONCEPTUAL DESIGN FORMAT SELECTION AID

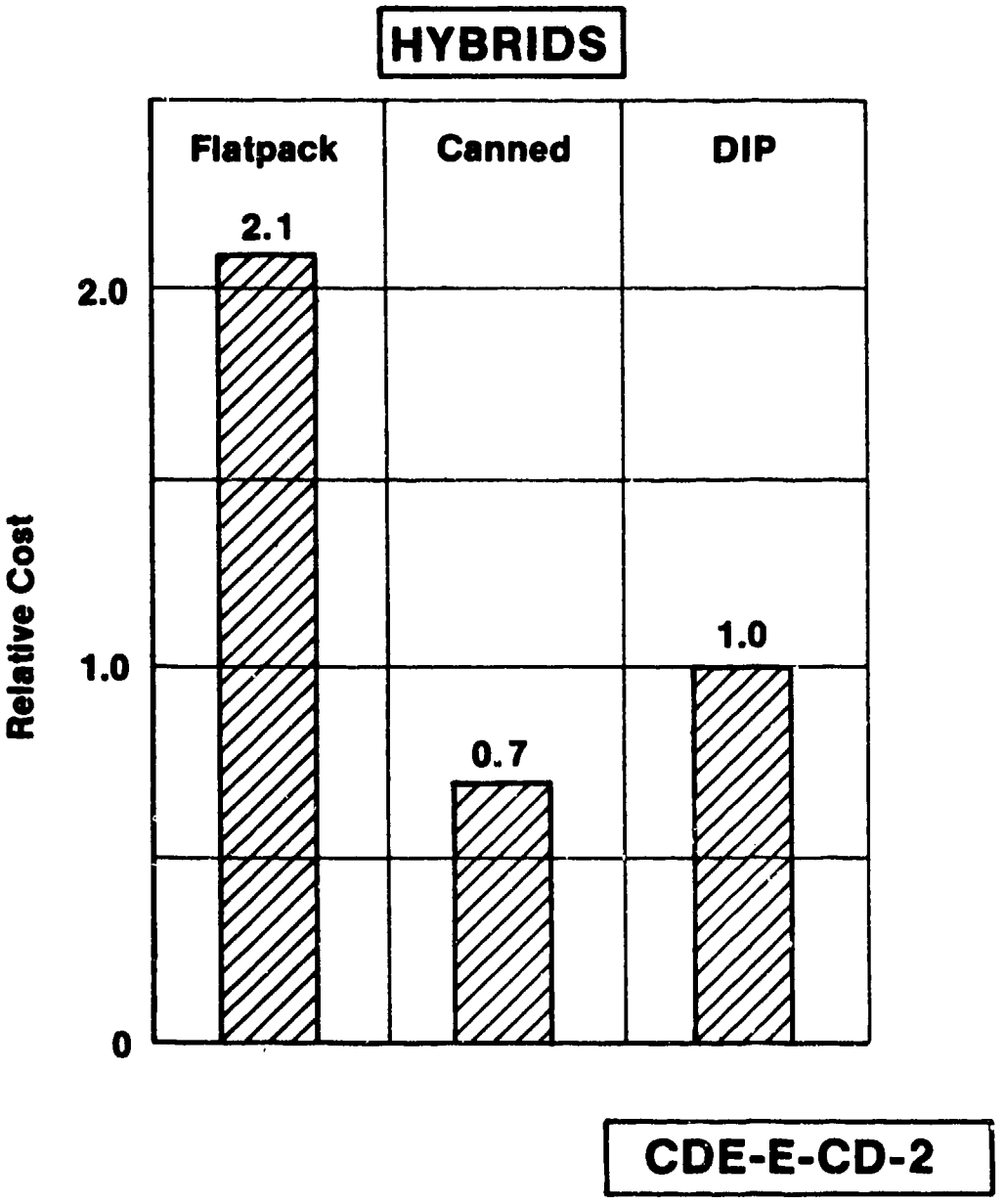
PART SELECTION (ELECTRICAL)
PACKAGE TYPE

CAPACITORS



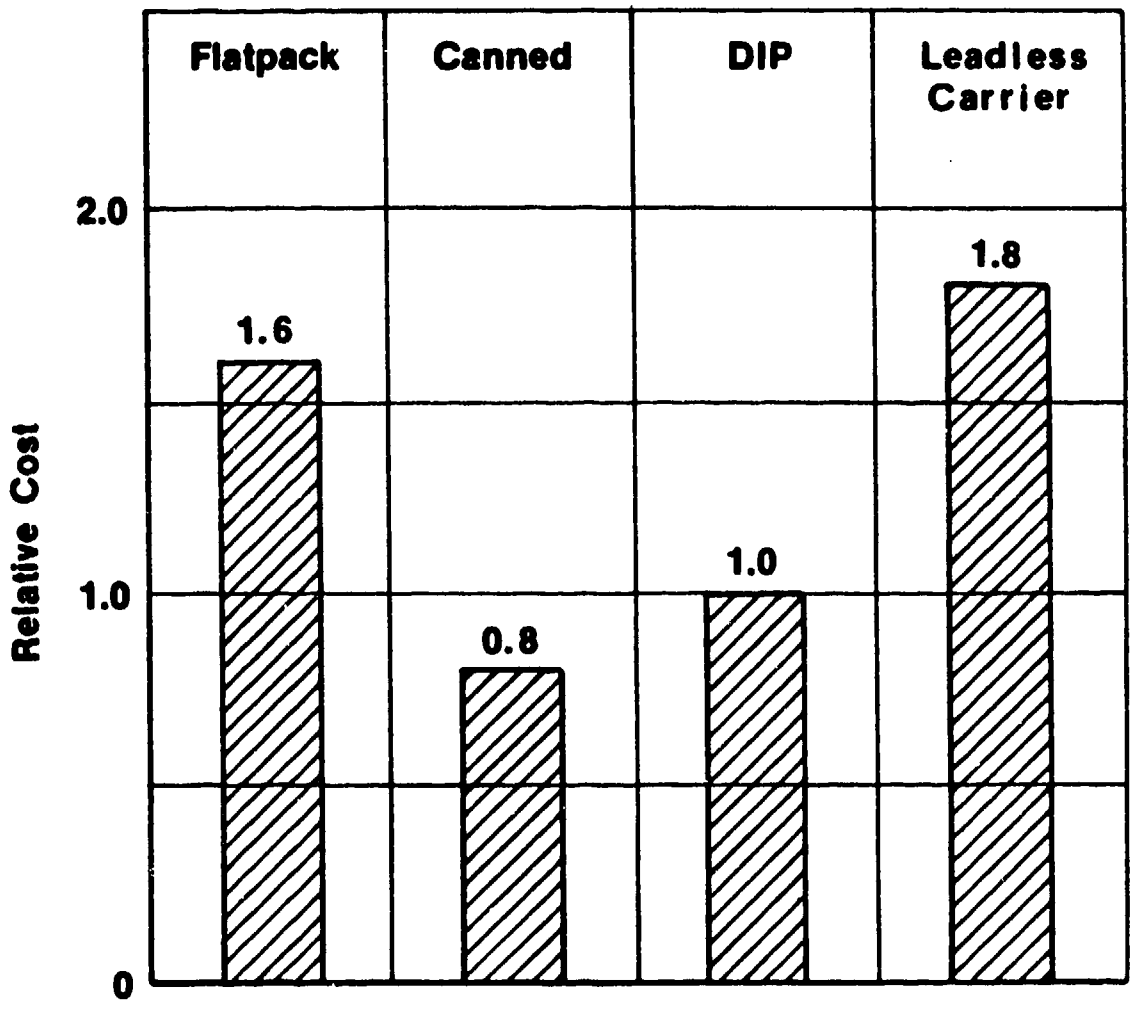
CDE-E-CD-1

PART SELECTION (ELECTRICAL)
PACKAGE TYPE



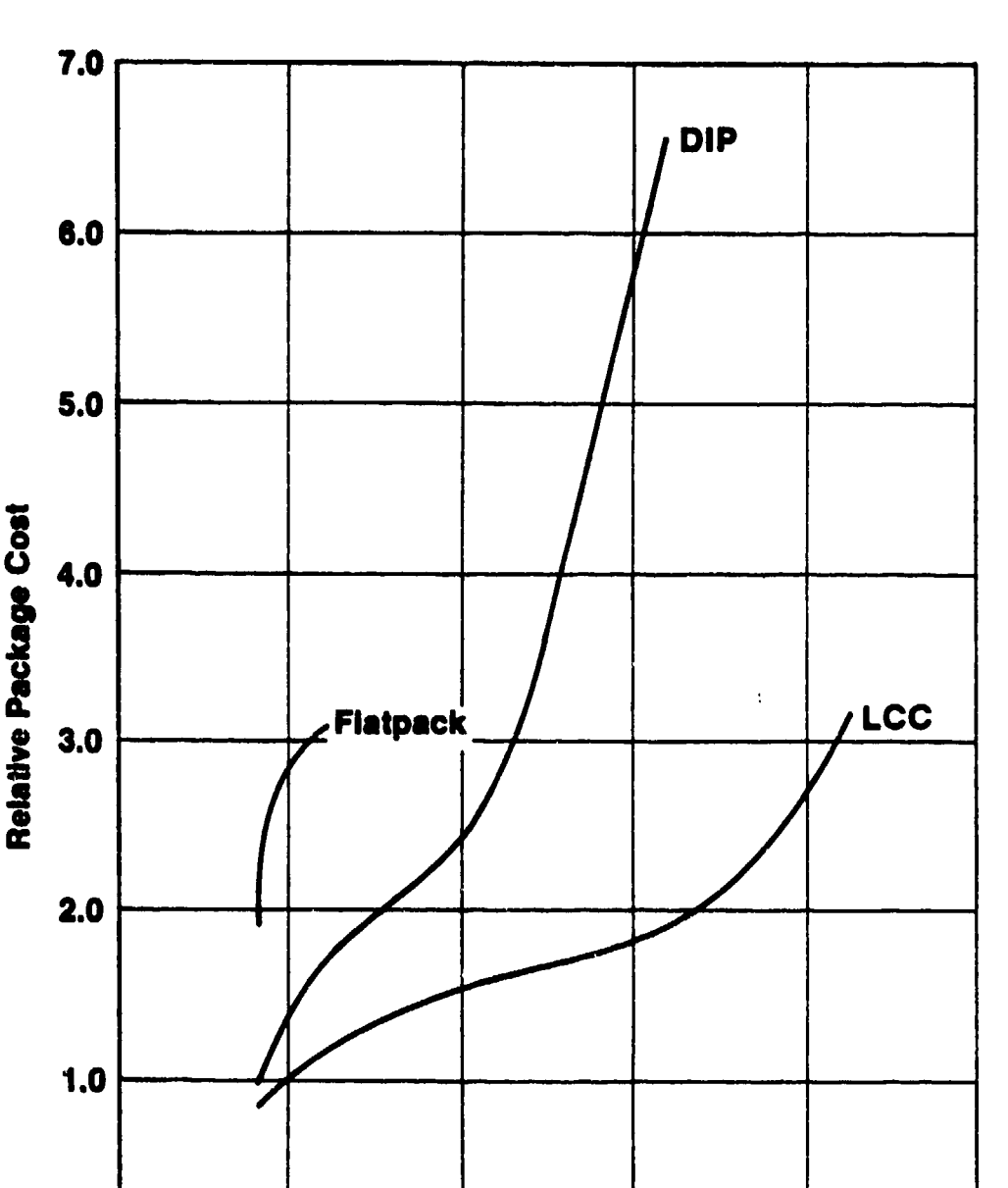
PART SELECTION (ELECTRICAL)
PACKAGE TYPE

INTEGRATED CIRCUITS



CDE-E-CD-3

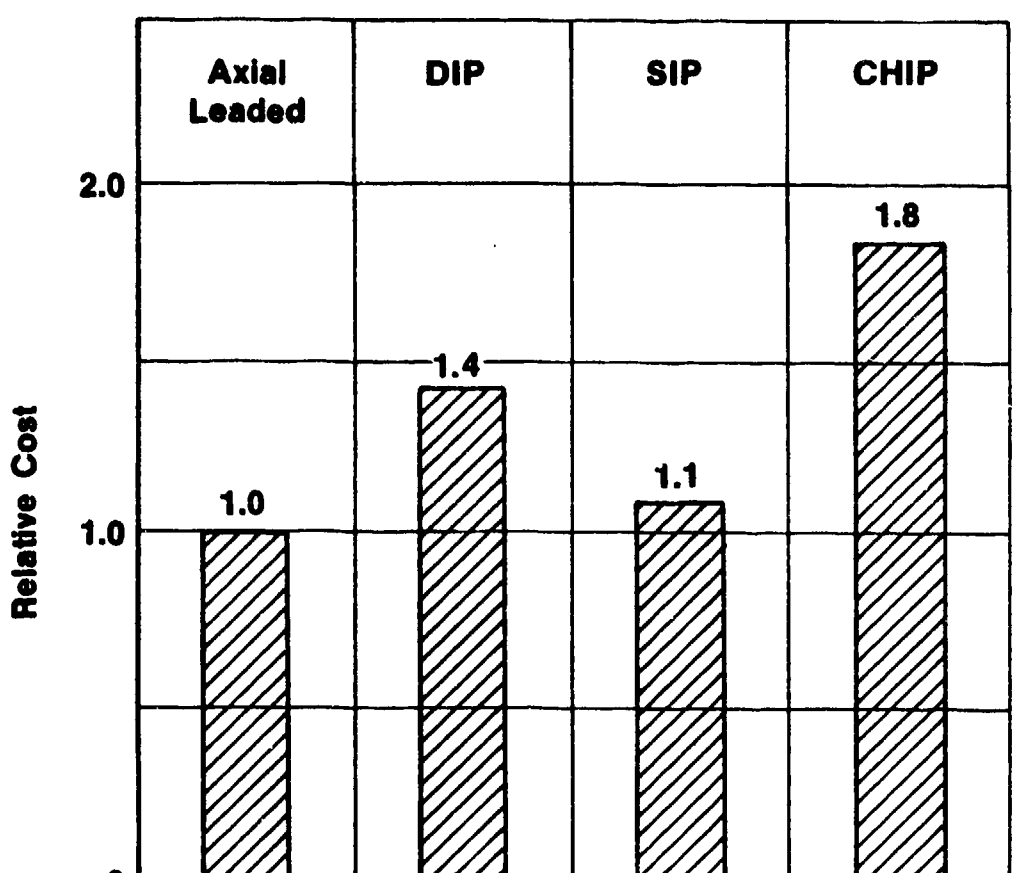
I.C. PACKAGE COST VS. NUMBER OF PIN-OUTS



CDE-E-CD-4

PART SELECTION (ELECTRICAL)
PACKAGE TYPE

RESISTORS



CDE-E-CD-5

4.2.8 Part Selection - Reliability Section

This section contains the format selection aid and formats for part selection (electrical) and presents the cost of achieving various reliability levels when complying with different specifications. Examples of electronic parts considered are switching diodes, rectifiers, and capacitors. The formats presented in this section include cost-driver effects (CDE) and cost estimating data (CED).

4.2.8.1 Format Selection Aid

The format selection aid (Figure 4-18) indicates all the formats that can be utilized in the conceptual design process. Those providing cost information on reliability are indicated by the shaded box.

Some formats will be applicable at both the conceptual and detail design phases of electronic systems.

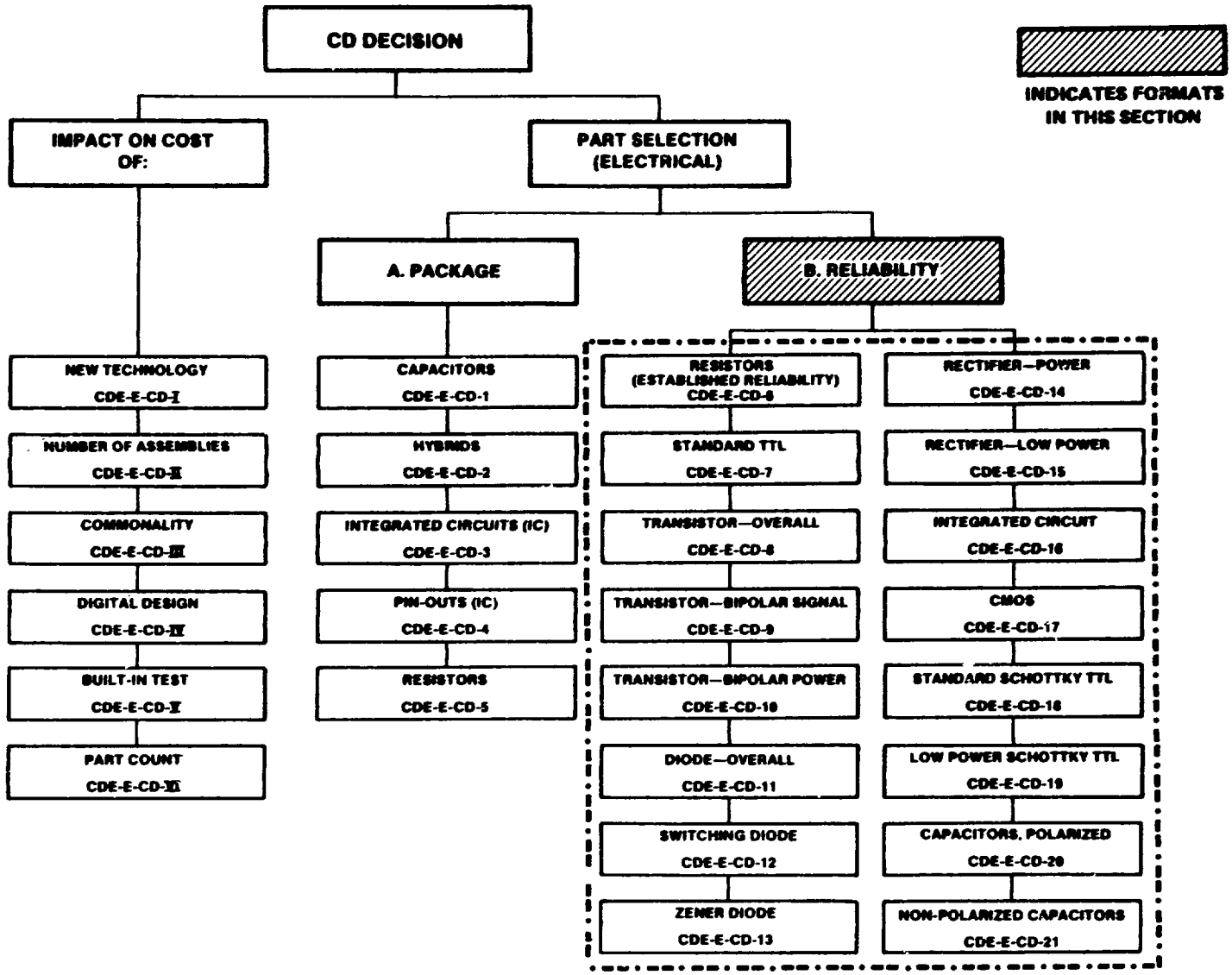


FIGURE 4-18. CONCEPTUAL DESIGN FORMAT SELECTION AID

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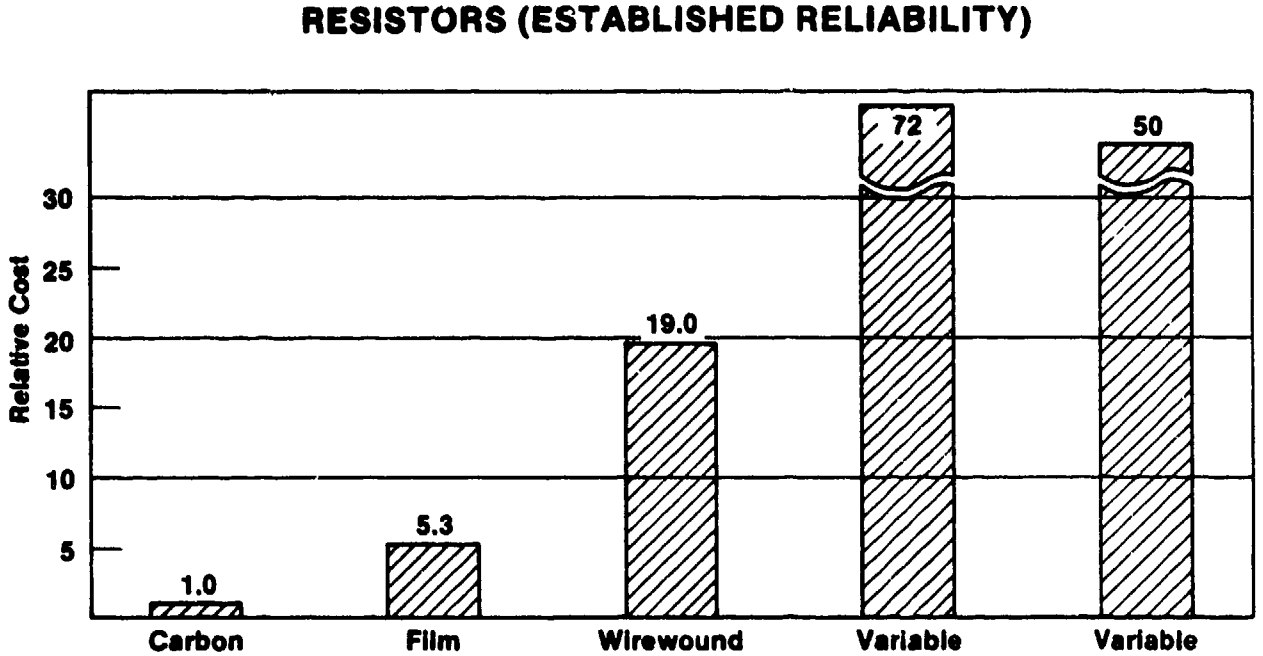
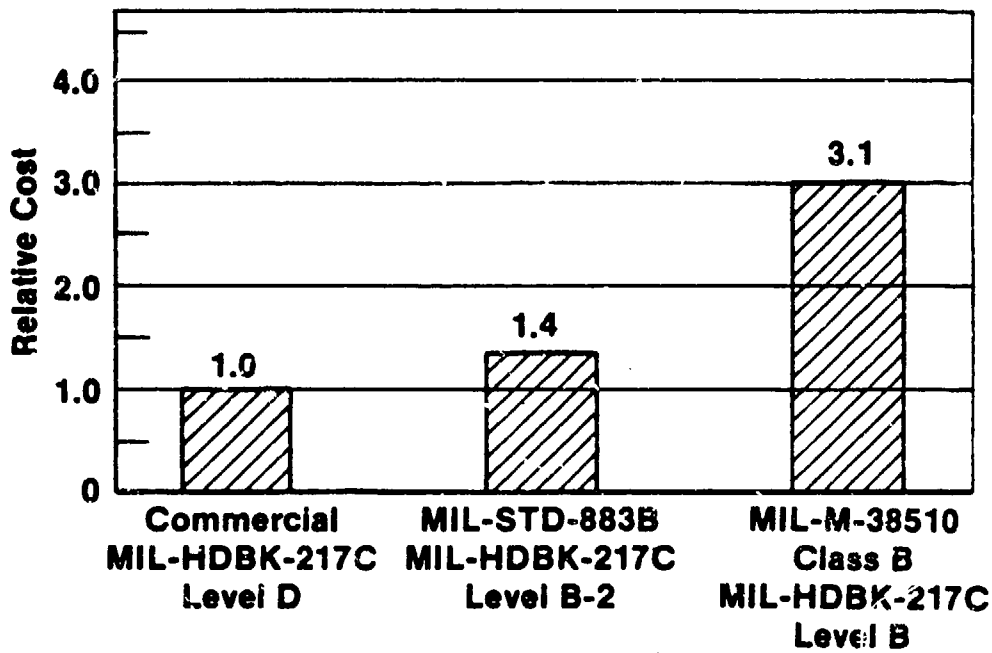
RESISTORS (ESTABLISHED RELIABILITY)

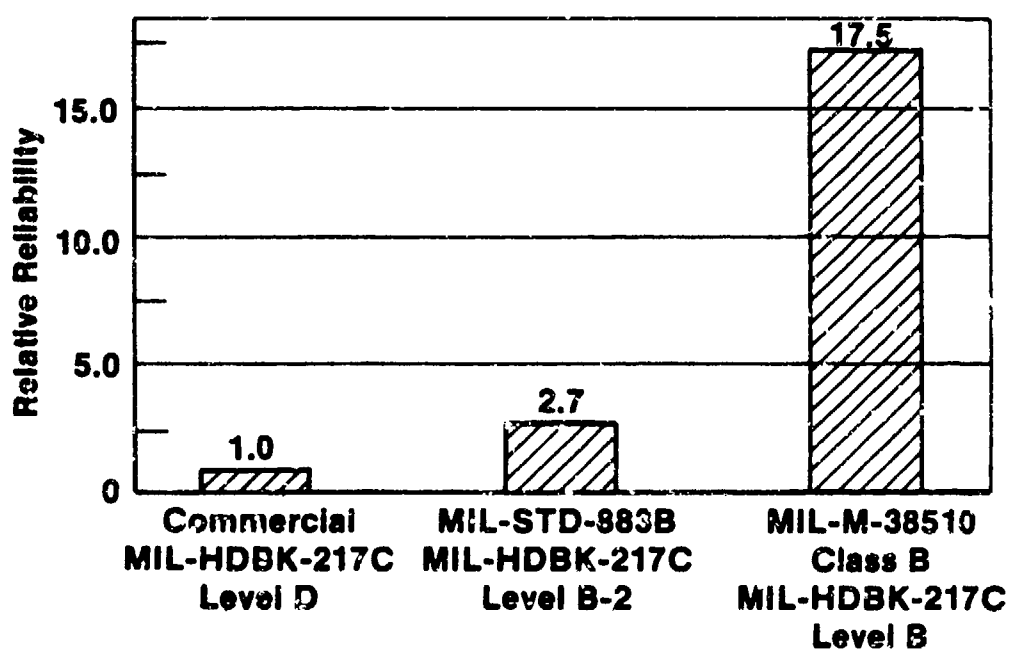


CDE-E-CD-6

STANDARD TTL

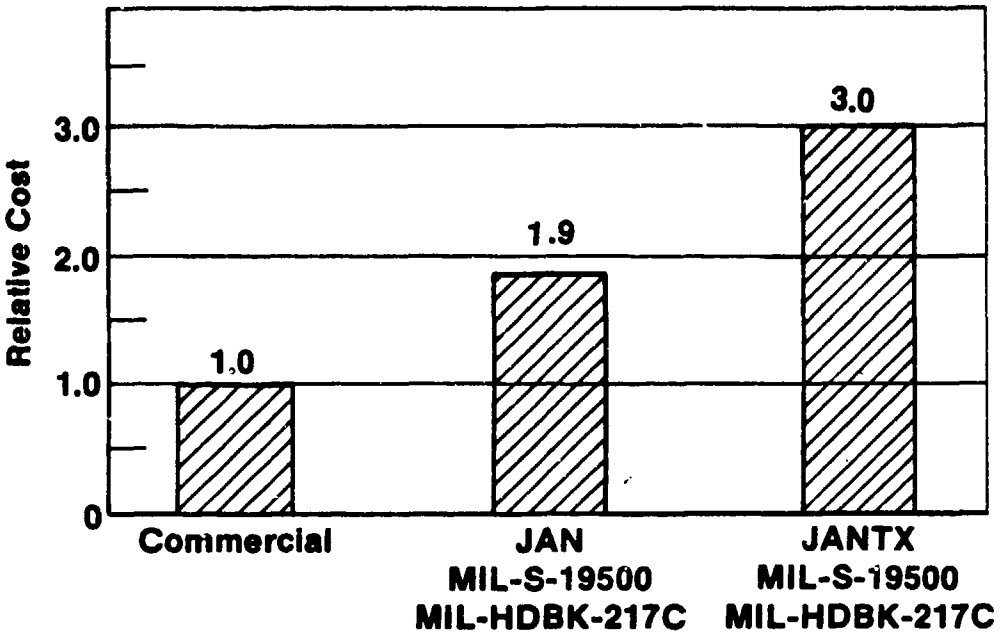


STANDARD TTL

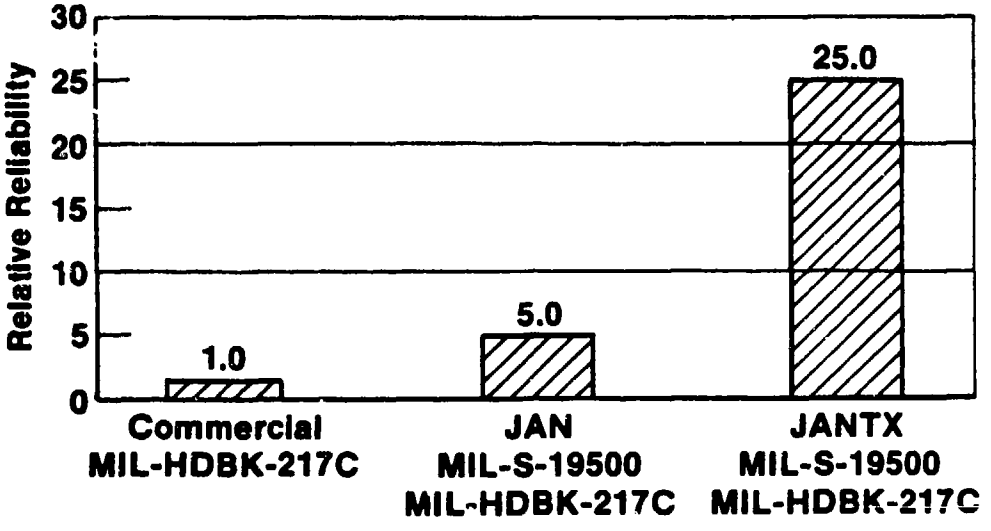


CDF-E-CD-7

TRANSISTOR — OVERALL

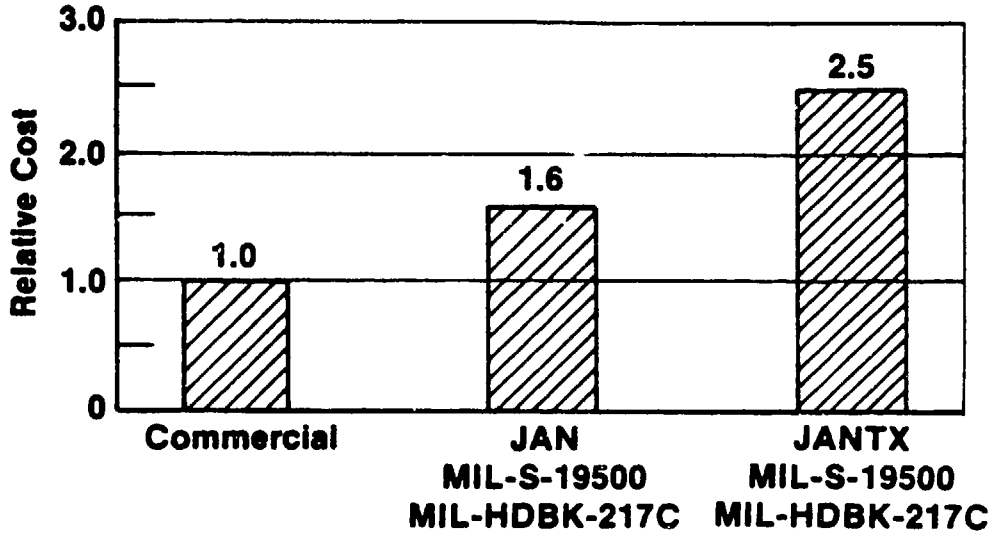


TRANSISTOR — OVERALL

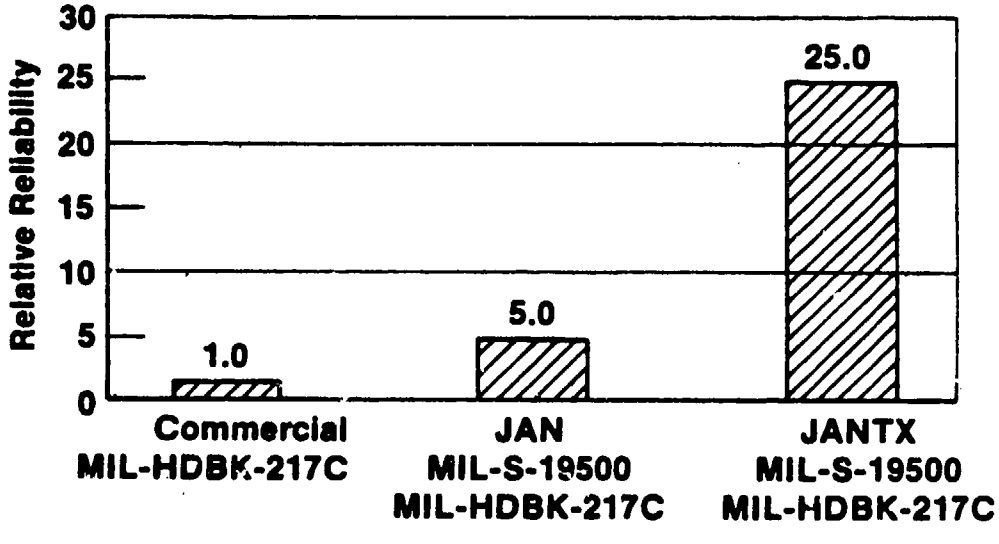


CDE-E-CD-8

TRANSISTOR — BIPOLAR SIGNAL

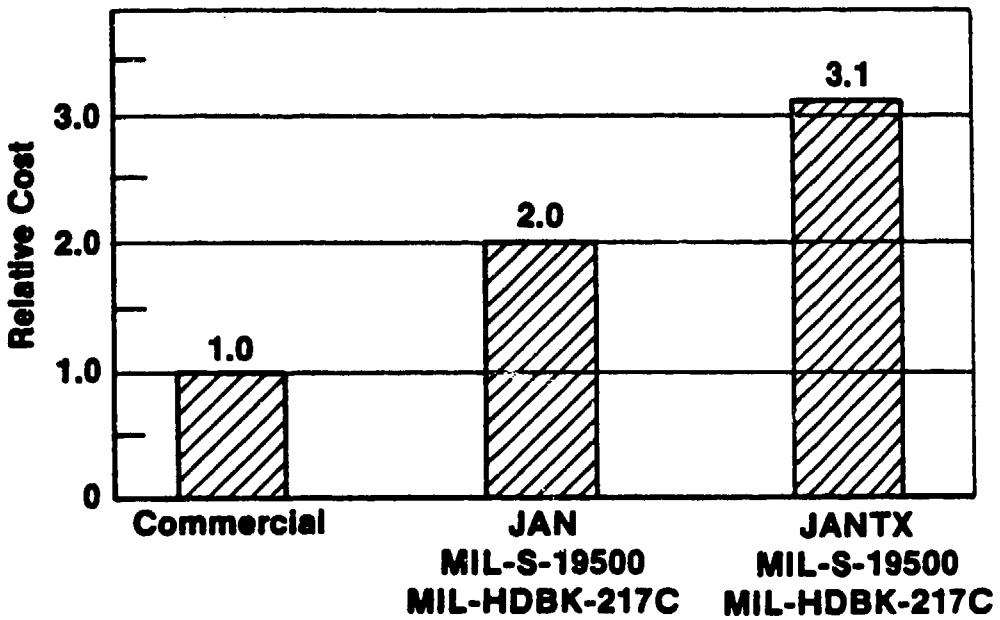


TRANSISTOR — BIPOLAR SIGNAL

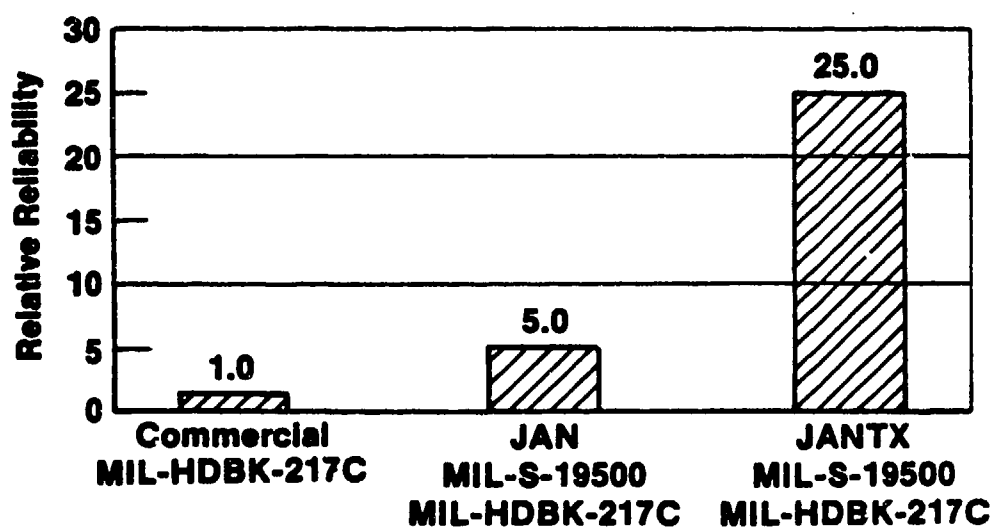


CDE-E-CD-9

TRANSISTOR — BIPOLAR POWER

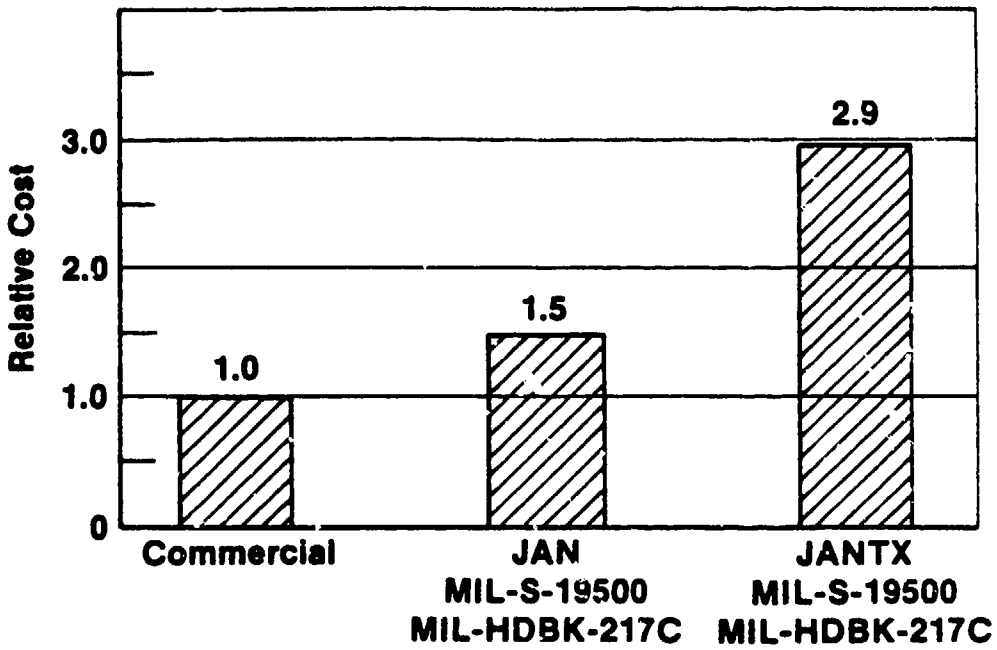


TRANSISTOR — BIPOLAR POWER

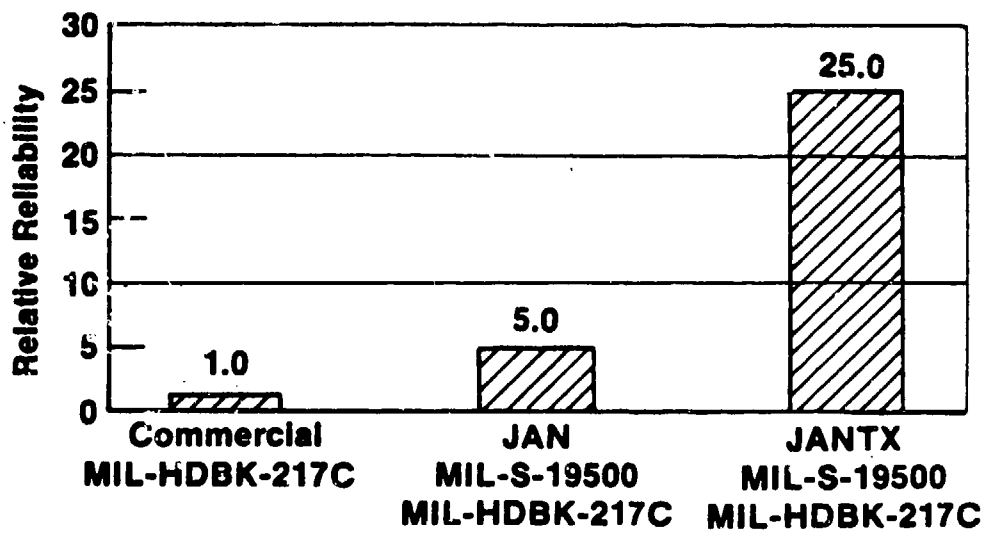


CDE-E-CD-10

DIODE — OVERALL

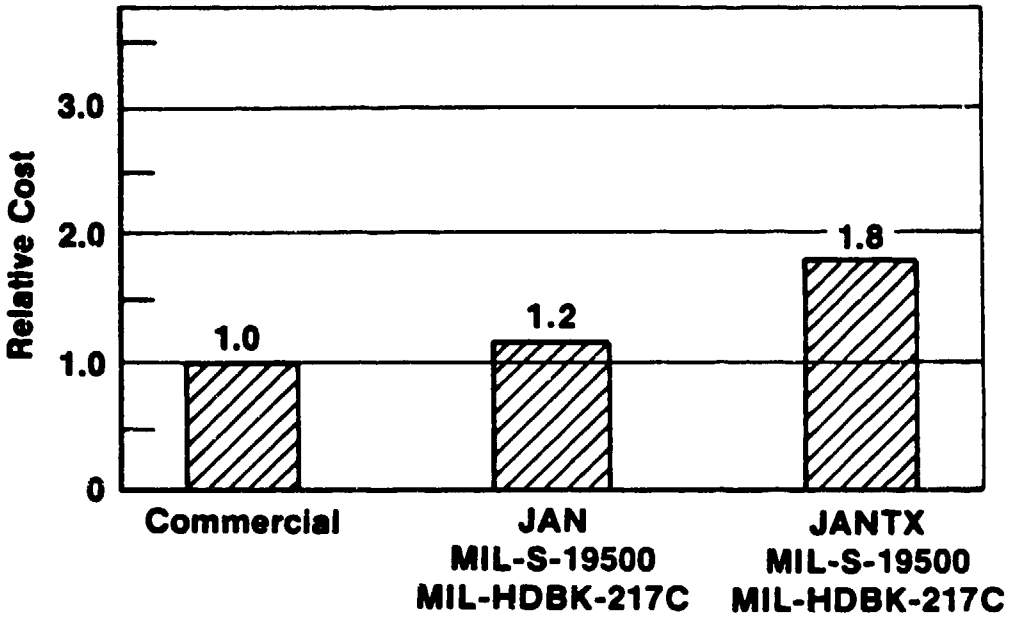


DIODE — OVERALL

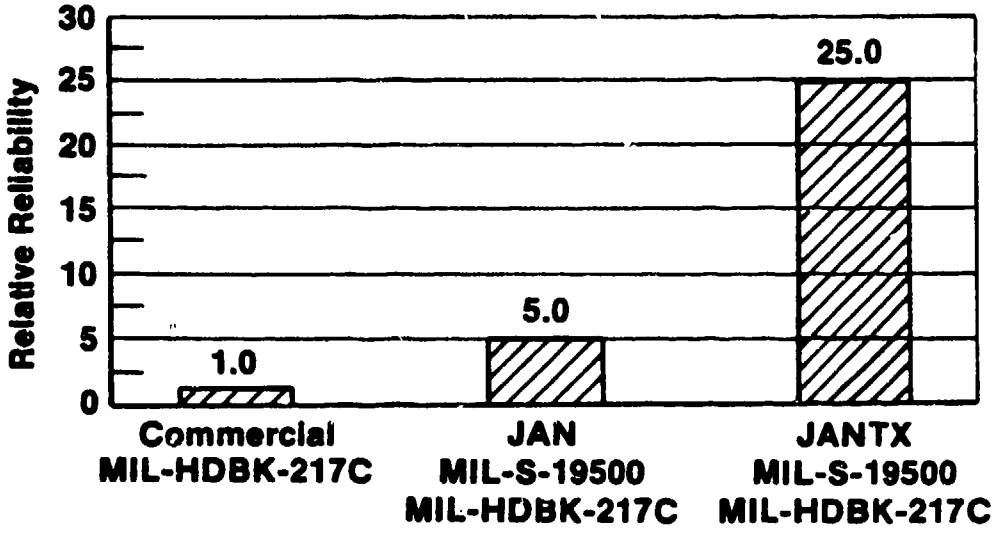


CDE-E-CD-11

SWITCHING DIODE

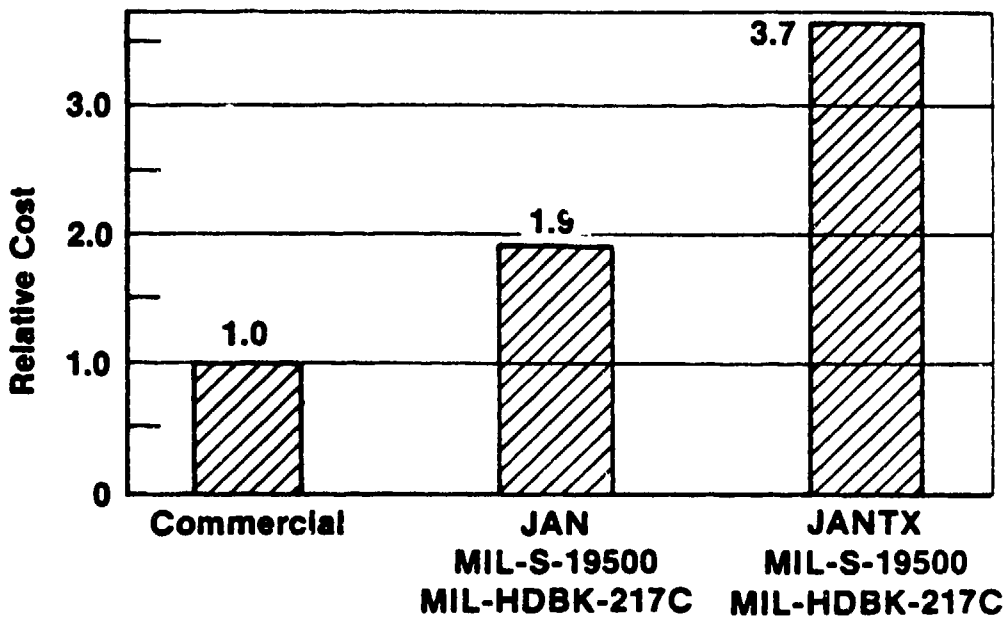


SWITCHING DIODE

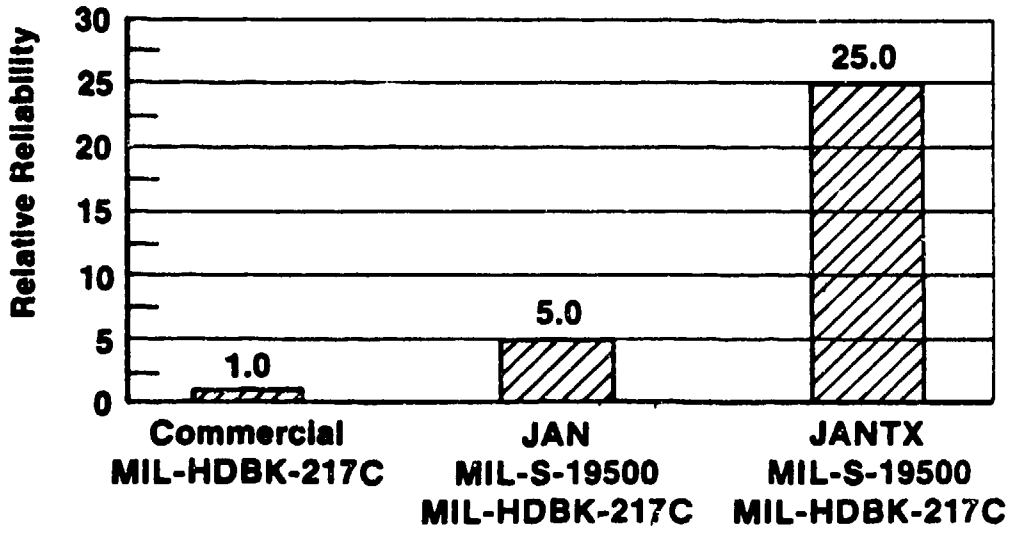


CDE-E-CD-12

ZENER DIODE

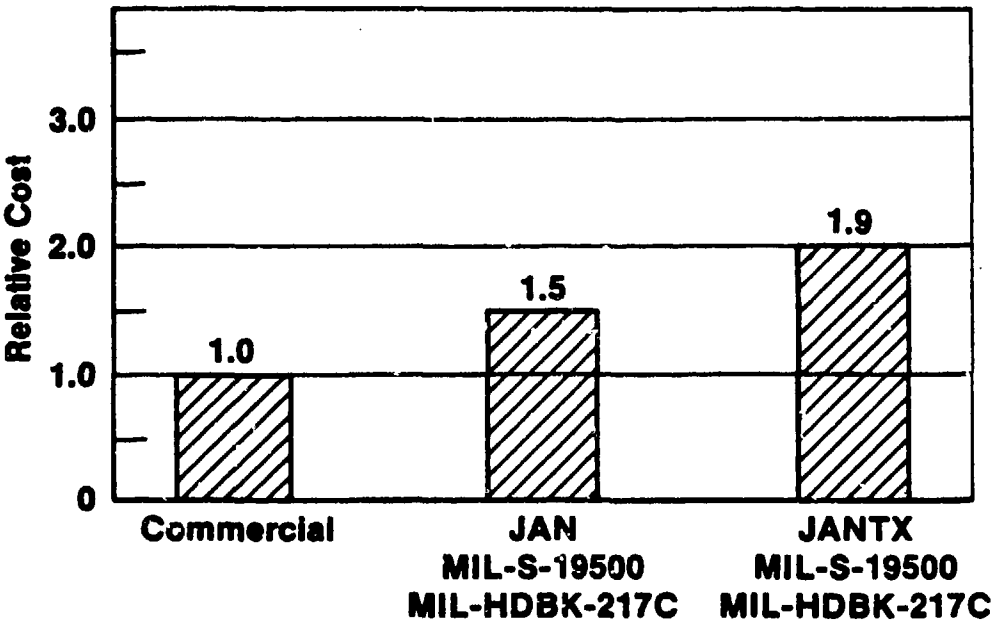


ZENER DIODE

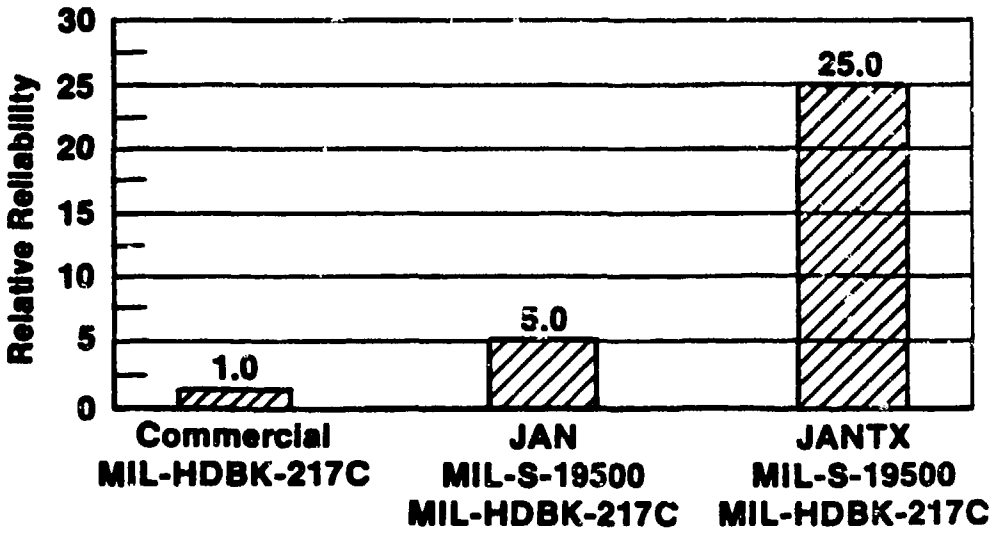


CDE-E-CD-13

RECTIFIER — POWER

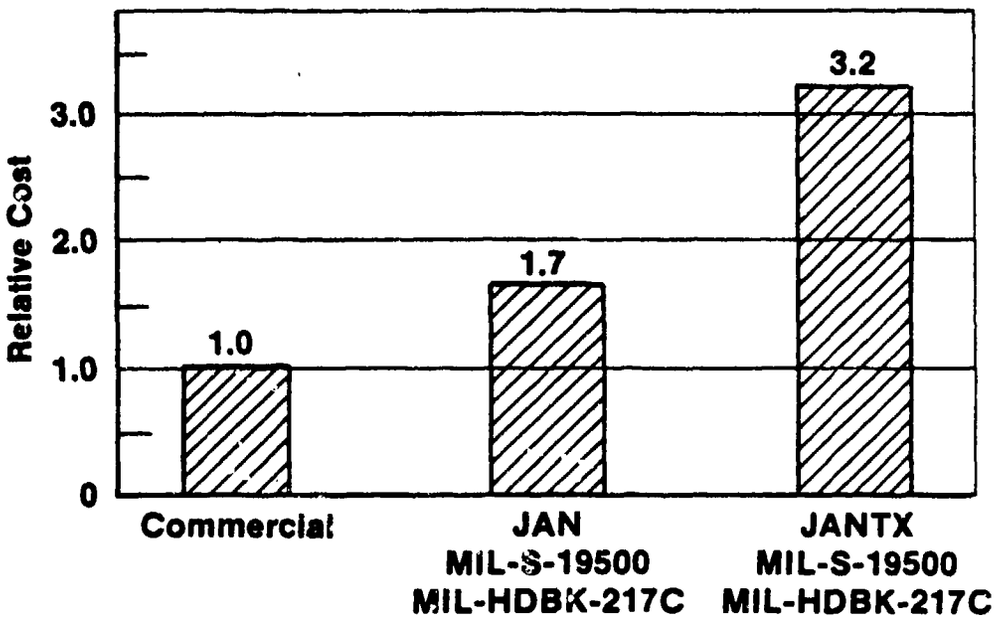


RECTIFIER — POWER

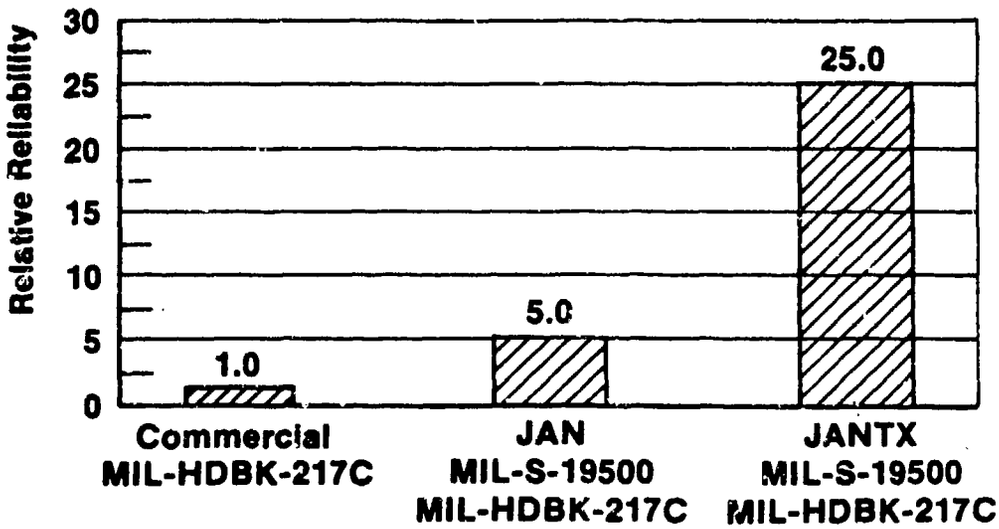


CDE-E-CD-14

RECTIFIER — LOW POWER

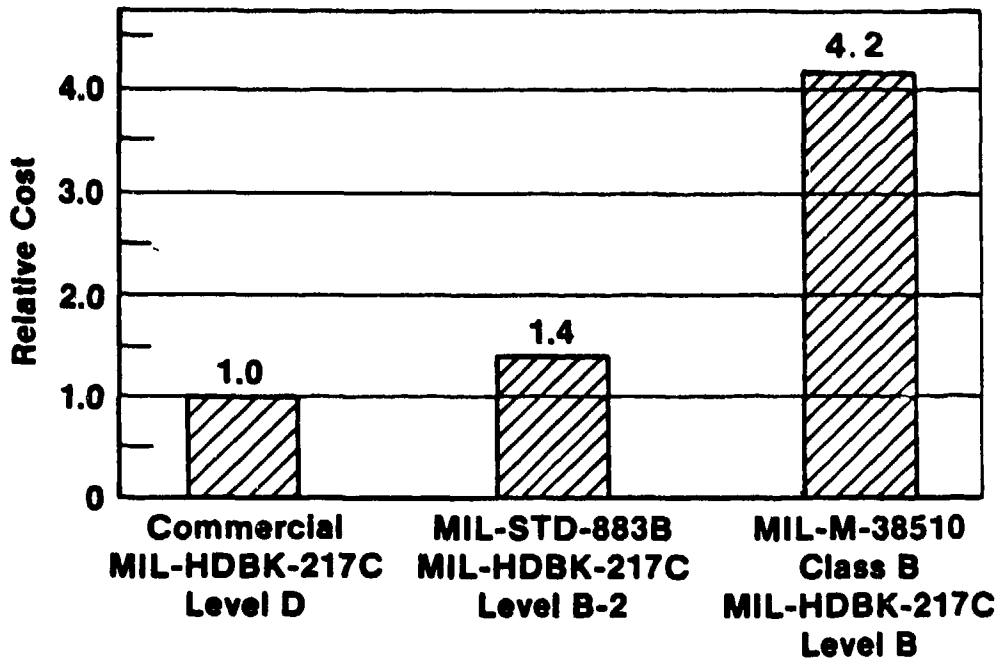


RECTIFIER — LOW POWER

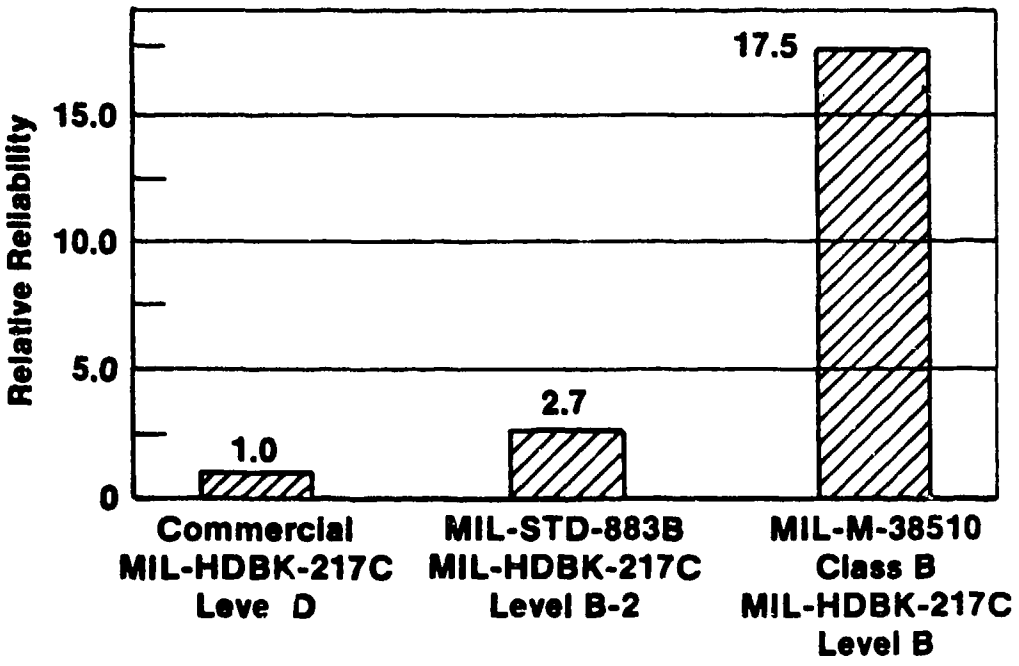


CDE-E-CD-15

INTEGRATED CIRCUIT, DIGITAL-COMPOSITE

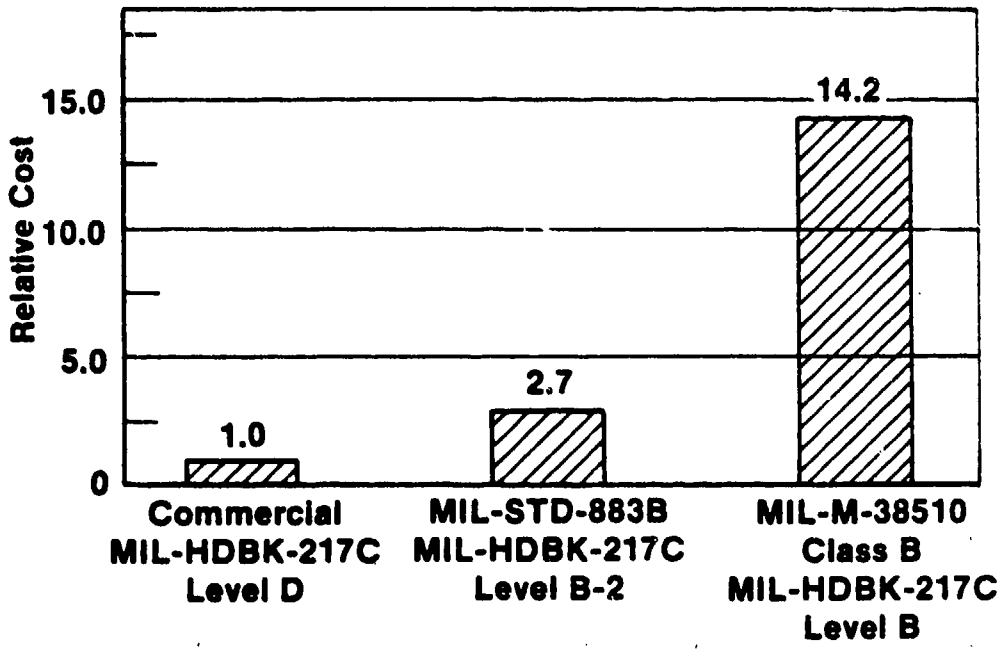


INTEGRATED CIRCUIT, DIGITAL-COMPOSITE

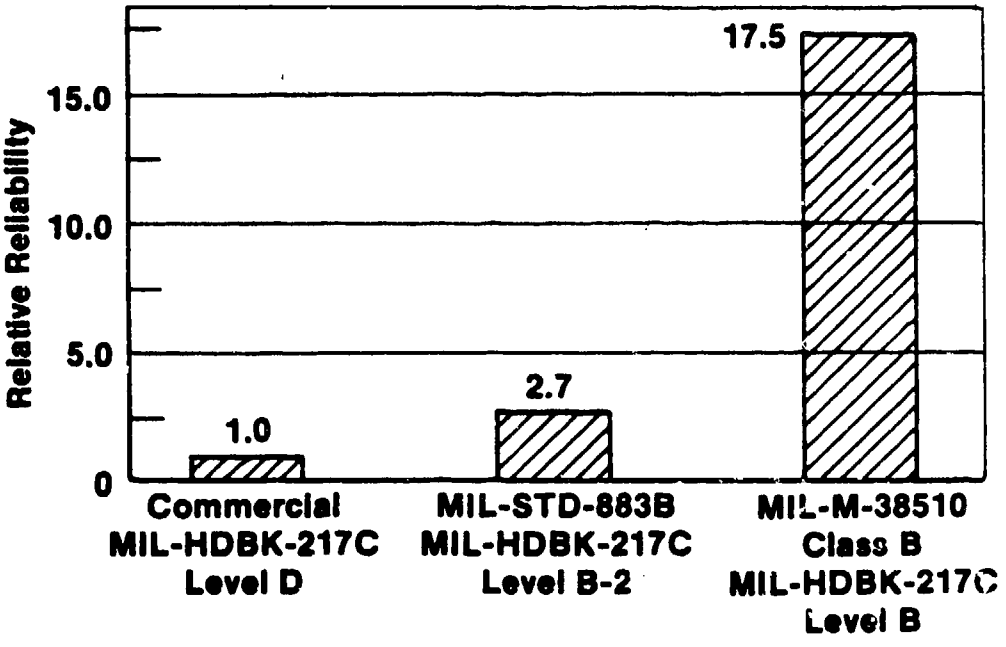


CDE-E-CD-16

CMOS

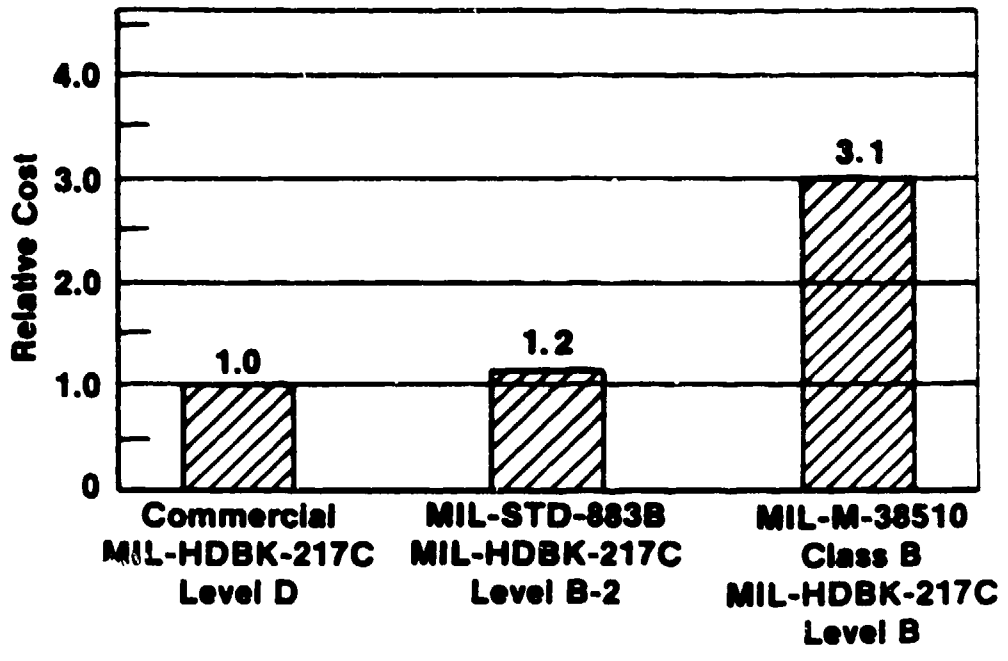


CMOS

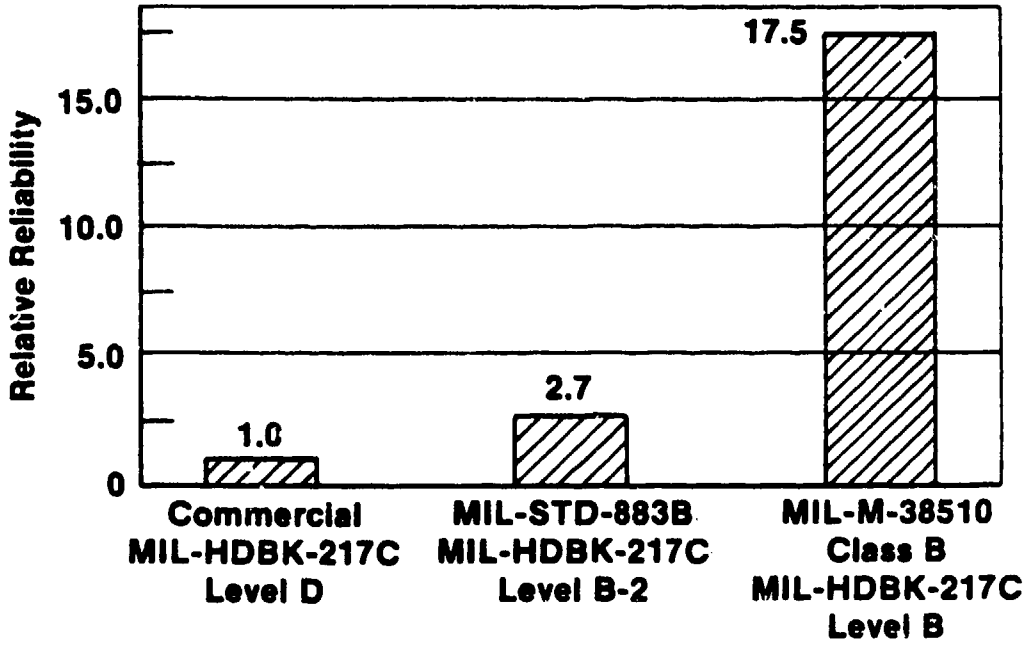


CDE-E-CD-17

STANDARD SCHOTTKY TTL

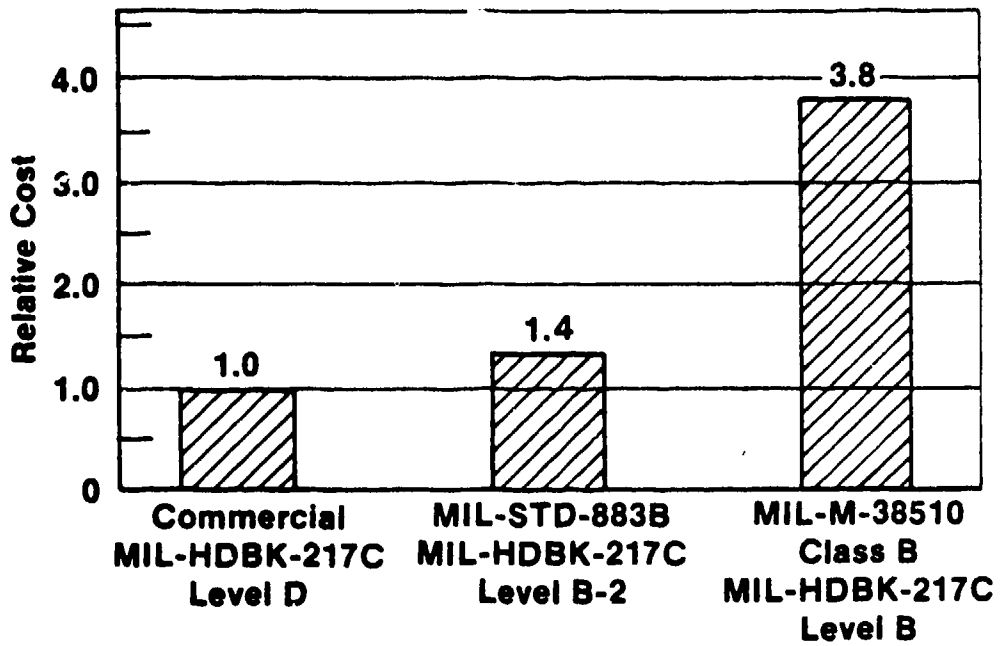


STANDARD SCHOTTKY TTL

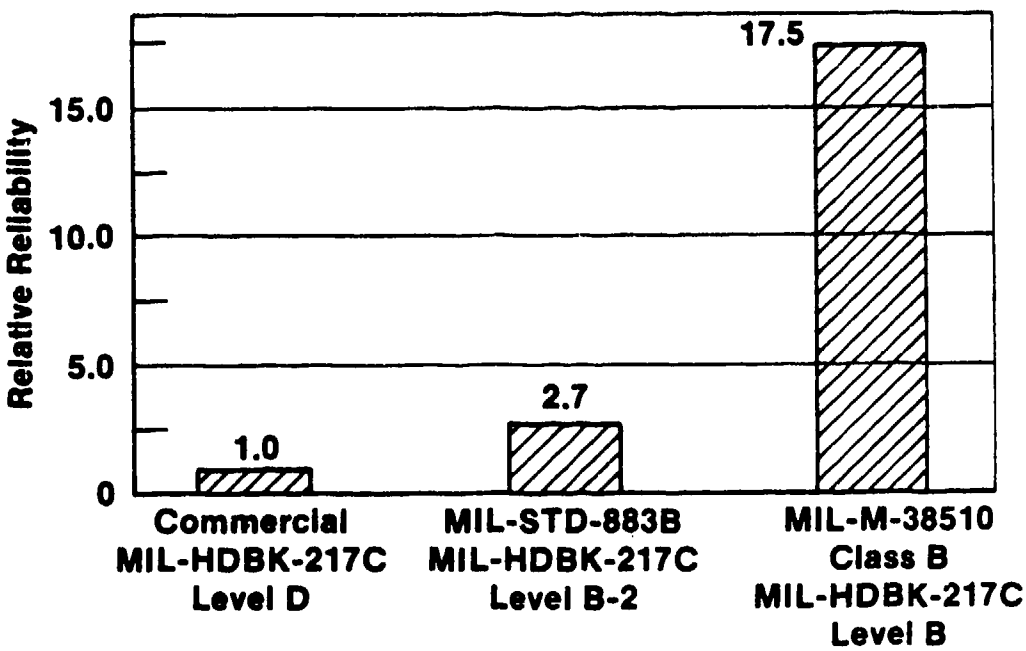


CDE-E-CD-18

LOW POWER SCHOTTKY TTL

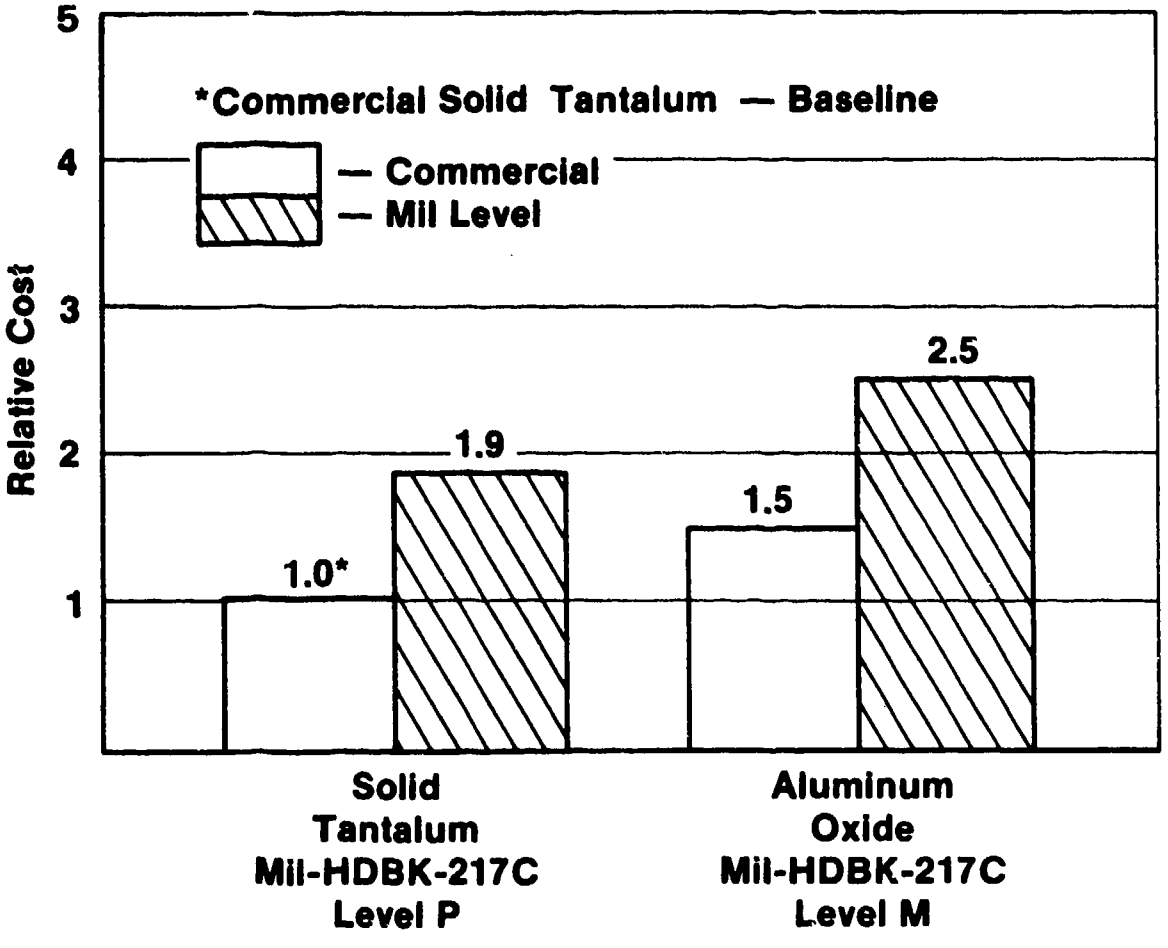


LOW POWER SCHOTTKY TTL



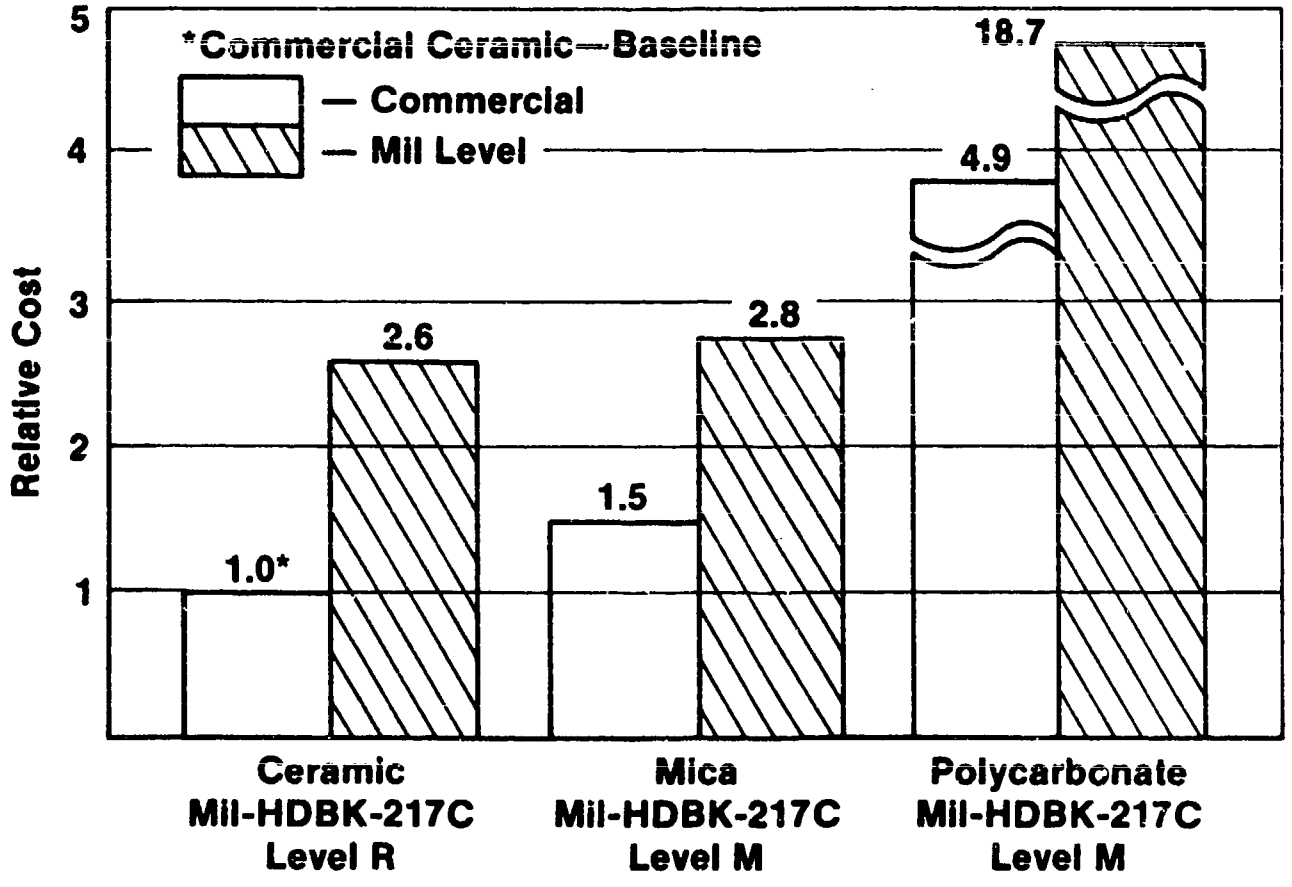
CDE-E-CD-19

CAPACITORS, POLARIZED



CDE-E-CD-20

NON-POLARIZED CAPACITORS



CDE-E-CD-21

SECTION 5
DETAIL DESIGN

5.1 Background

Information about the detail design (DD) phase is shown in Figures 1-1 and 3-1. The former figure indicates that while the leverage to reduce cost is more significant at the conceptual design (CD) phase, DD still presents an important opportunity to minimize cost. Figure 3-1 shows that, using the cost estimating data (CED) formats for the circuit and mechanical elements of the electronic system, minimized manufacturing cost can be achieved prior to design review.

The formats on the following pages provide the detail designer of electronics with material and manufacturing cost guidance that enables trade-offs to be conducted between design objectives and manufacturing cost for:

- Mechanization
- Processes
- Insertion (PWA)
- Soldering (PWA).

5.2 Utilization Example for Printed Wiring Assembly

This example demonstrates how the data generated are utilized on a specific detail design problem. The example shows how to identify applicable formats and extract data from them, and provides a discussion on how the data are used to determine the part cost in man-hours or dollars. The MC/DG cost worksheets can be used to record the cost data for easy reference and to determine the total program cost. The worksheets are included as Tables 5-1 through 5-5.

5.2.1 Problem Statement

This problem illustrates the procedure that a design engineer follows in conducting trade-off studies on a typical printed wiring assembly (PWA). The PWA chosen for the trade-off study is the power supply for an interface glideslope RF signal-to-noise-indicator. The complexity of the power supply is such that it is not necessary to conduct the custom versus discrete part trade.

5.2.2 Procedure

The design engineer reviews the Format Selection Aid (Figure 5-1) for Part Selection under Mechanization and can perform a number of trade-offs. For illustrative purposes, we assume that the design engineer is

interested in determining the impact of select versus variable resistors. Two potentiometers (variable resistors) are used on the power supply board. Using Figure 5-2 (CDE-E-DD-3), the material and the labor-cost differences are compared.

The detail design phase material worksheet utilized for the power supply PWA is included as Table 5-1.

Using the MC/DG Electronic Cost Worksheet (Table 5-2), a cost savings of 6.5 percent is calculated for using select rather than variable resistors. Quantified, this is $2.80 per PWA. However, the labor cost must also be determined.

With the assumption that the normalized cost is $0.60 for the variable resistor assembly labor, the cost difference is computed as follows:

Select Labor Cost:

$$[(1.5)\ \$0.60 + (5.3\text{-}1.5)\ \$8.82] \times 2.0 = \$6.36$$

Variable Labor Cost:

$$[(1.1)\ \$0.60 + (2.3\text{-}1.1)\ \$8.82] \times 2.0 = \$2.76$$

Thus, the labor cost savings of $3.60 per PWA, using the potentiometer, outweighs the $2.80 material cost savings using the select resistor. Different labor rates and different material costs may produce results that favor the select resistors.

Referring to the Detail Design Process Selection Aid, Figure 5-3 (CDE-E-DD-5) is used to select the type of packages. G-10 material and polyimide are considered, with the less costly G-10 selected by the designers because very high temperature operation is not required.

Reviewing the package types listed on Figure 5-3 (CDE-E-DD-5) and the insertion process selection chart on Figure 5-4 (CDE-E-DD-6), an insertion problem for the flatpack device is revealed. Hand insertion is the only standard process that can be used, and this is a high-cost process. Using the same procedure for the soldering process, the selection chart, Figure 5-5 (CDE-E-DD-7), shows the wave-soldering for flatpacks will require special processing.

Other package types for the integrated circuit should be explored to select one that can be inserted/soldered using standard processes. A review of this part (M38510/11502) indicates that a DIP version is also available. The DIP package will allow auto-insertion and wave-soldering with normal processing.

The part cost and the recurring labor cost differences must be determined to quantify the manufacturing cost impact. The MC/DG Electronic Cost Worksheet (Table 5-2) can be used to determine the cost impact for the package type change.

Labor Estimation Worksheets can be used to quantify the assembly labor difference (Tables 5-4 and 5-5).

The flatpack can be semi-auto-inserted, whereas the DIP can be auto-inserted. The difference is 3.59 man-hours per 1000 assemblies, a labor savings. The soldering difference is (4.20 - 6.33) = -2.13 man-hours per 1000 assemblies; a labor increase. Summation of the two results in a labor savings of 1.46 man-hours per 1000 assemblies. With an assembly labor rate of $6.74, the resultant cost savings is $9.84 per 1000 assemblies.

For this trade, the overall savings is $0.67 (piece part) + $0.01 (labor) or $0.68 per assembly.

The Labor Estimation worksheets for insertion and soldering in conjunction with the parts list can be used to determine the recurring assembly labor for the power supply assembly. Using the worksheets with the process selection aid, the assembly labor for insertion is 53.14 man-hours per 1000 assemblies and the assembly labor for soldering is 60.60 man-hours per 1000 assemblies. The total is 113.74 man-hours per 1000 assemblies using the applicable least-costly processes.

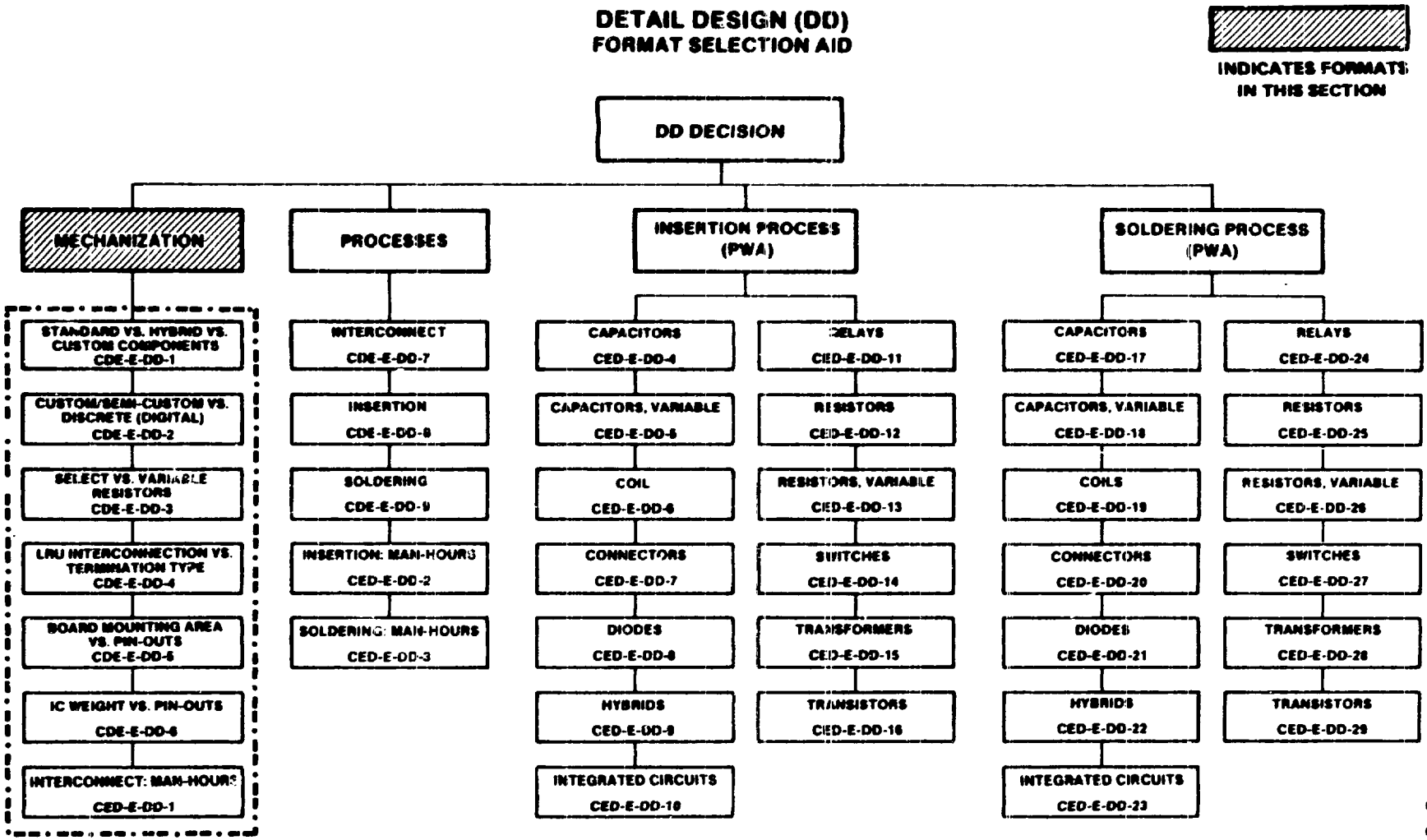


FIGURE 5-1. DETAIL DESIGN FORMAT SELECTION AID

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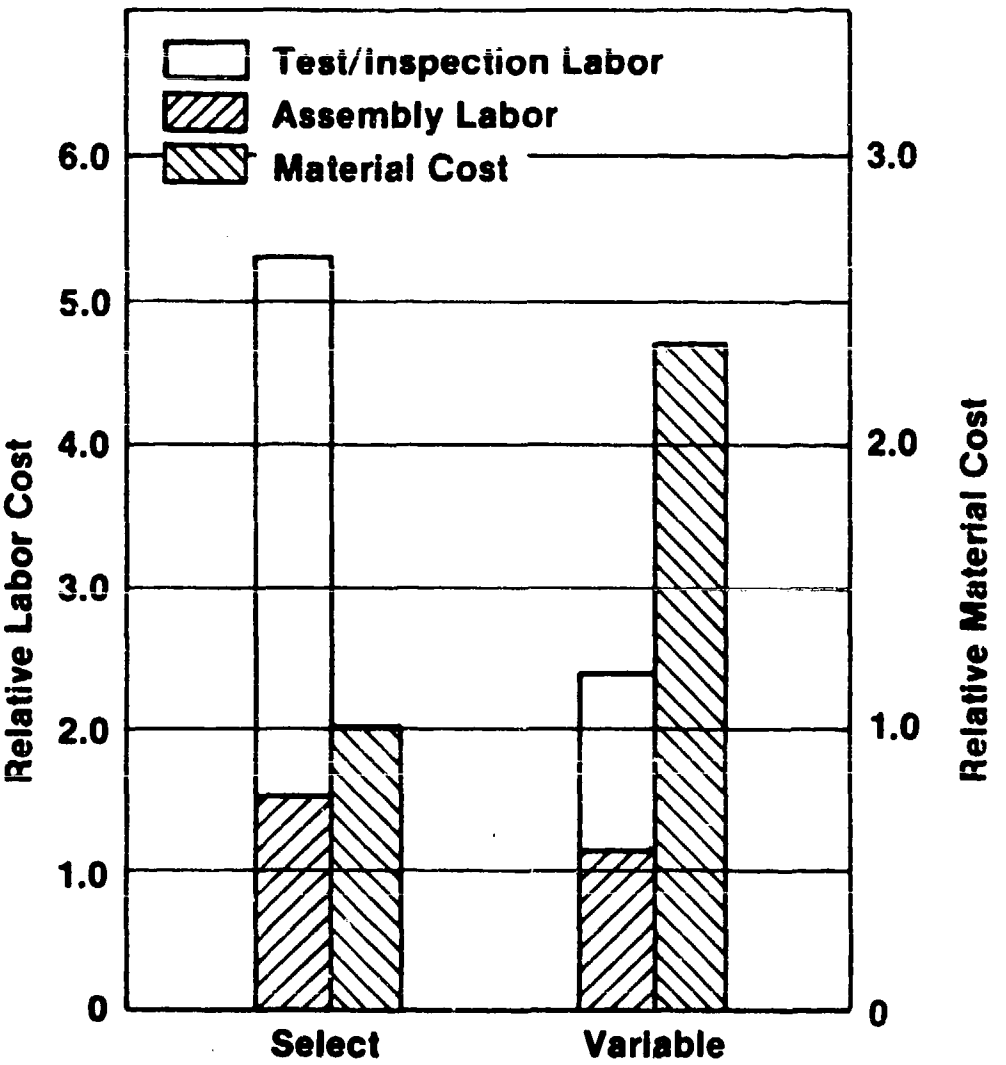
3 Jan 1983

MAN-HOURS/MATERIAL COST VS. RESISTOR TYPE



CDE-E-DD-3

FIGURE 5-2. FORMAT USED IN EXAMPLE

PROCESS/MATERIAL CONSIDERATIONS FOR INTERCONNECT BETWEEN COMPONENTS

PROCESS	Polymide	G-10	Teflon	Ceramic	Multi-Wire
PART PACKAGE SUITABILITY					
Conventional Leaded	A	A	S	S	S
Beam Ribbon	S	A	S	A	N
Leadless	S	N	N	A	N
INSERTION/ATTACHMENT					
Hand	A	A	S	A	S
Semi-Auto	A	A	S	A	S
Auto	A	A	S	A	S
SOLDERING					
Hand	A	A	S	A	S
Wave	A	A	S	N	S
Vapor	S	S	S	A	S
Infrared	S	S	N	S	S
Laser	S	S	N	N	S

A Applicable

S Applicable (May Require Special Processing/Equipment)

N Not Applicable

CDE-E-DD-5

FIGURE 5-3. FORMAT USED IN EXAMPLE

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

RELATIVE COST	LOW	MEDIUM	HIGH
INSERTION PROCESS	Auto	Semi-Auto	Hand
PART TYPE			
RESISTORS			
Axial Leaded	A	A	A
DIP	S	A	A
SIP	N	A	A
Chip	A	S	A
VARIABLE RESISTORS			
Sealed	N	A	A
Open	N	A	A
CAPACITORS			
Axial Leaded	A	A	A
Radial Leaded	A	A	A
DIP	A	A	A
SIP	N	A	A
Chip	A	S	A
VARIABLE CAPACITORS			
Opened	N	A	A
Sealed	N	A	A
COILS			
Axial Leaded	S	A	A
Variable	N	N	S
DIODES	A	A	A
TRANSISTORS			
Standard Leaded	N	A	A
Ribbon Leaded	N	N	A

A Applicable
S Applicable (May Require Special Processing/Equipment)
N Not Applicable

CDE-E-DD-6

FIGURE 5-4. FORMAT USED IN EXAMPLE

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED) (CONTINUED)

RELATIVE COST	LOW	MEDIUM	HIGH
INSERTION PROCESS	Auto	Semi-Auto	Hand
PART TYPE			
INTEGRATED CIRCUITS			
Flatpacks	N	S	A
Canned	N	A	A
DIP	S	A	A
Leadless Carrier (28 Pin-Out)	A	S	A
MIP (100 Pin-Out)	N	A	A
HYBRIDS			
Flatpacks	N	S	A
Canned	N	A	A
DIP	A	A	A
MIP (28 Pin-Out)	N	A	A
SWITCHES	N	N	A
TRANSFORMERS	N	N	A
RELAYS	N	N	A
CONNECTORS			
Circular	N	N	A
Printed Circuit	N	N	A
Square Pin	A	A	A

A Applicable
S Applicable (May Require Special Processing/Equipment)
N Not Applicable

CDE-E-DD-6

FIGURE 5-4. FORMAT USED IN EXAMPLE (Continued)

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)

RELATIVE COST	LOW	LOW	MEDIUM	MEDIUM	HIGH
SOLDERING PROCESS	Infrared*	Laser*	Wave	Vapor Phase*	Hand
PART TYPE					
RESISTORS					
Axial Leaded	A	A	A	A	A
DIP	A	A	A	A	A
SIP	A	A	A	A	A
Chip	A	N	A	A	S
VARIABLE RESISTORS					
Sealed	A	A	A	A	A
Open	A	S	N	N	A
CAPACITORS					
Axial Leaded	A	A	A	A	A
Radial Leaded	A	A	A	A	A
DIP	A	A	A	A	A
SIP	A	A	A	A	A
Chip	A	N	A	A	S
VARIABLE CAPACITORS					
Sealed	A	A	A	A	A
Open	S	N	N	N	A
COILS					
Axial Leaded	A	A	A	A	A
Variable	S	N	A	A	S
DIODES	N	N	A	A	A
TRANSISTORS					
Standard Leaded	A	A	A	A	A
Ribbon Leaded	A	N	N	A	A

*Pre-Applied Solder/Flux Required

A Applicable

S Applicable (May Require Special Processing/Equipment)

N Not Applicable

CDE-E-DD-7

FIGURE 5-5. FORMAT USED IN EXAMPLE

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED) (CONTINUED)

RELATIVE COST	LOW	LOW	MEDIUM	MEDIUM	HIGH
SOLDERING PROCESS	Infrared*	Laser*	Wave	Vapor Phase*	Hand
PART TYPE					
INTEGRATED CIRCUITS					
Flatpacks	A	A	S	A	A
Canned	A	A	A	A	A
DIP	A	A	A	A	A
Leadless Carrier (28 Pin-Out)	A	N	N	A	N
MIP (100 Pin-Out)	A	N	A	A	A
HYBRIDS					
Flatpacks	A	A	S	A	A
Canned	A	A	A	A	A
DIP	A	A	A	A	A
Leadless Carrier (28 Pin-Out)	A	N	N	A	N
MIP (100 Pin-Out)	A	N	A	A	A
SWITCHES	N	A	N	N	A
TRANSFORMERS	N	N	S	N	A
RELAYS	N	S	S	N	A
CONNECTORS					
Circular	S	N	S	S	A
Printed Circuit	N	N	A	N	A
Square Pin	A	A	S	A	A

*Pre-Applied Solder/Flux Required

A Applicable

S Applicable (May Require Special Processing/Equipment)

N Not Applicable

CDE-E-DD-7

FIGURE 5-5. FORMAT USED IN EXAMPLE
(Continued)

TABLE 5-1

MATERIAL WORKSHEET

ICAM "MANUFACTURING COST/DESIGN GUIDE (MC/DG)"
FOR ELECTRONICS AND FABRICATION ASSEMBLY

ASSEMBLY TYPE: Power Supply **LOT SIZE:** 20

VENDOR PART NUMBER	PART DESCRIPTION	QUANTITY PER ASSEMBLY	PACKAGE TYPE	COST $/PART	NON-RECURRING VENDOR COST/MAN HOURS	RECURRING COST $/ASSEMBLY	% OF TOTAL COST
M38510/11502	Integrated Circuit	1	F/P	1.50		1.50	3.5
JTX2N3055	Transistor	1	CAN STD	1.18		1.18	2.7
JTX2N2222A	Transistor	2	CAN STD	0.25		0.50	1.2
JTX1N645-1	Diode	2	Axial	0.20		0.40	0.9
JTX1N4454-1	Diode	2	Axial	0.20		0.40	0.9
M39018/03-0743	Capacitor, Elect	2	Axial	1.97		3.94	9.1
M390M/02-1230	Capacitor, Cer.	4	Radial	0.25		1.00	2.3
RJR24FP501M	Potentiometer	2	—	2.35		4.70	10.9
—	Transformer	1	—	9.50		9.50	22.0
—	Inductor	3	Axial	2.73		8.19	19.0
—	PWB (4x4) (2 Layer)	1	—	9.07	290.00	9.07	21.0
BERG 65002-75	Connector (25 contacts)	1	—	2.50		2.50	5.8
RCR 07G2200JS	Resistor, Carbon	2	Axial	0.03		0.06	0.2
RCR 07G1103JS	Resistor, Carbon	3	Axial	0.04		0.12	0.3
RCR 07G0053JS	Resistor, Carbon	3	Axial	0.03		0.09	0.2
SUMMATION		30				43.15	100.0

TABLE 5-2

MC/DG ELECTRONIC DESIGNER'S COST WORKSHEET

Baseline Configuration: Interface Assembly LRU
Indenture Level: RF Module Subassembly SRU

Baseline Manufacturing Cost Allocation: $ 43.15

DESIGN DECISION: Part Selection	1	2	3	4	5	6	7
Piece Part Type	% Total Electronic Part Cost	Baseline Approach	Reference	Study Approach	Ratio: Baseline to Study Approaches	Cost Factor (%) (1 ÷ 5)	Cost* Change (%) (1 - 6)
RESISTOR, VARIABLE	10.9	POT	CDE-5-DD-3	TEST SELECT	2.5	4.4	+6.5
INTEGRATED CIRCUIT	3.5	FLATPACK	CDE-5-CD-3	DIP	1.8	1.9	+1.6

Total +8.1

Cost Impact: Baseline Manufacturing Cost ($) x Cost Change Total (%) = ($) 43.15 x 8.1 (%: Total of Column 7) = ($) 3.50

New Cost: Baseline Manufacturing Cost ($) - Cost Impact = ($) 43.15 - ($) 3.50 = ($) 39.65

*Notes: Positive Value = Cost Savings
Negative Value = Cost Increase

Remarks _____

By: J. Vecellio
Date: 15 Sept. 1981

FTR450252000U
3 Jan 1983

TABLE 5-3. INSTRUCTIONS FOR USING COST WORKSHEET

Step	Column	Input	Procedure
1	1	% of total electronic parts cost	Determine portion of electronic parts cost in each category (Column 1 will not necessarily total 100%).
2	2	Baseline approach	List baseline electronic components, e.g., flatpack.
3	3	Reference formats	From "MC/DG for Electronics", e.g., CDE-E-DD-3.
4	4	Study approach	Cost area investigated for selection of electronic components, e.g., DIP.
5	5	Ratio of baseline to study	Divide baseline approach factor from reference format by study approach factor.
6	6	Cost factor (%)	Divide Column 1 by Column 5.
7	7	Cost change (%)	Column 1 minus Column 6 (enter + and - signs for summation and decision). Positive indicates reduced expense. Negative indicates increased cost.
8			Repeat steps 1 through 7 for each piece part type.
9			Total Column 7 and observe sign.
10			Multiply total from Step 9 by total cost of electronic parts to determine change in cost between baseline and study approach of electronic parts.

TABLE 5-4

INSERTION LABOR ESTIMATION WORKSHEET

ASSEMBLY NAME: POWER SUPPLY SHEET 1 OF 2

	COLUMN			1	2		
	INSERTION PROCESS				PROCESS ALTERNATIVES		
	MAN-HOURS PER 1000				EXTENDED MAN-HOURS PER 1000		
PART TYPE	AUTO	SEMI-AUTO	HAND	QUANTITY PER ASSEMBLY	AUTO	SEMI-AUTO	HAND
RESISTORS							
Axial-Leaded	0.29	2.39	2.94	8	2.32		
DIP	0.44	4.44	4.74				
SIP	N/A	3.00	3.34				
Chip	0.47	1.20	2.10				
VARIABLE RESISTORS							
Sealed	N/A	4.00	4.59				
Open	N/A	4.00	4.59	2			9.18
CAPACITORS							
Axial Leaded	0.29	2.39	2.94	2	0.58		
Radial Leaded	0.29	2.89	3.14	4	1.16		
DIP	0.44	4.40	4.74				
SIP	N/A	3.00	3.34				
Chip	0.47	1.20	2.10				
VARIABLE CAPACITORS							
Sealed	N/A	2.34	2.59				
Open	N/A	2.34	2.59				
COILS							
Axial Leaded	0.25	2.39	2.94	3	0.75		
Variable	N/A	N/A	2.50				
DIODES	0.25	1.83	2.33	4	1.00		
	SHEET 1 SUMMATION				5.81		9.18
	PROCESS ALTERNATIVES				AUTO	SEMI-AUTO	HAND

TABLE 5-4

INSERTION LABOR ESTIMATION WORKSHEET (Continued)

ASSEMBLY NAME: POWER SUPPLY SHEET 2 OF 2

	COLUMN			1	2		
	INSERTION PROCESS				PROCESS ALTERNATIVES		
	MAN-HOURS PER 1000				EXTENDED MAN-HOURS PER 1000		
PART TYPE	AUTO	SEMI-AUTO	HAND	QUANTITY PER ASSEMBLY	AUTO	SEMI-AUTO	HAND
TRANSISTORS							
Standard Leaded	N/A	3.74	4.20	3			12.60
Ribbon Leaded	N/A	N/A	7.83				
INTEGRATED CIRCUIT							
Flatpacks	N/A	5.80	4.32				
Canned	N/A	6.95	7.84				
DIP	0.44	4.40	4.74	1	0.44		
Leadless Carrier	0.55	8.00	7.67				
MIP							
HYBRIDS							
Flatpacks	N/A	5.80	4.32				
Canned	N/A	6.95	7.84				
DIP	0.44	4.40	4.74				
Leadless Carrier							
SWITCHES	N/A	N/A	4.37				
TRANSFORMERS	N/A	N/A	5.17	1			5.17
RELAYS	N/A	N/A	5.07				
CONNECTORS* (100 PIN)							
Circular	N/A	N/A	118.35				
Printed Circuit	N/A	N/A	79.75	1(25 PINS)			19.94
Square Pin	13.33	60.00	86.65				
SHEET 2 SUMMATION					0.44		37.71
SHEET 1 SUMMATION					5.81		9.18
TOTAL SUMMATION					6.25		46.89
PROCESS ALTERNATIVES					AUTO	SEMI-AUTO	HAND

*Normalize for less than 100 pins.

TABLE 5-5

SOLDERING LABOR ESTIMATION WORKSHEET

ASSEMBLY NAME: POWER SUPPLY SHEET 1 OF 2

	COLUMN					1	2				
	SOLDERING PROCESS MAN-HOURS PER 1000						PROCESS ALTERNATIVES EXTENDED MAN-HOURS PER 1000				
PART TYPE	H	W	Vφ	IR	L	QUANTITY PER ASSEMBLY	H	W	Vφ	IR	L
RESISTORS											
Axial-Leaded	3.90	0.84	0.64	0.60	0.60	8		6.72			
DIP	25.32	6.33	4.79	4.80	4.80						
SIP	13.18	3.57	2.75	2.40	2.40						
Chip	15.54	0.60	0.65	0.60	N/A						
VARIABLE RESISTORS											
Sealed	5.88	1.88	1.57	0.90	0.90						
Open	5.88	N/A	N/A	0.90	0.90	2	11.76				
CAPACITORS											
Axial-Leaded	3.90	0.84	0.64	0.60	0.60	2		1.68			
Radial Leaded	3.90	0.84	0.64	0.60	0.60	4		3.36			
DIP	25.32	6.33	4.79	4.80	4.80						
SIP	13.18	3.57	2.75	2.40	2.40						
Chip	15.54	0.60	0.65	0.60	N/A						
VARIABLE CAPACITORS											
Sealed	4.70	1.88	1.57	0.90	0.90						
Open	4.60	N/A	N/A	0.90	N/A						
COILS											
Axial-Leaded	3.90	0.84	0.64	0.60	0.60	3		2.52			
Variable	4.67	1.80	1.19	0.80	N/A						
DIODES	4.60	1.08	0.67	N/A	N/A	4		4.32			
	SHEET 1 SUMMATION						11.76	18.60			
	PROCESS ALTERNATIVES						H	W	Vφ	IR	L

TABLE 5-5

SOLDERING LABOR ESTIMATION WORKSHEET (Continued)

ASSEMBLY NAME: POWER SUPPLY SHEET 2 OF 2

	COLUMN					1	2				
	SOLDERING PROCESS						PROCESS ALTERNATIVES				
	MAN-HOURS PER 1000						EXTENDED MAN-HOURS PER 1000				
PART TYPE	H	W	Vφ	IR	L	QUANTITY PER ASSEMBLY	H	W	Vφ	IR	L
TRANSISTORS											
Standard Leaded	5.40	1.40	1.09	0.90	0.90	3		4.20			
Ribbon Leaded	7.71	N/A	2.62	1.30	N/A						
INTEGRATED CIRCUIT											
Flatpacks	25.67	4.20	4.20	4.20	4.20						
Canned	13.18	3.57	2.75	2.40	2.40						
DIP	25.32	6.33	4.79	4.80	4.80	1		6.33			
Leadless Carrier	N/A	N/A	8.54	10.00	N/A						
MIP											
HYBRIDS											
Flatpacks	25.67	4.20	4.20	4.20	4.20						
Canned	13.18	3.57	2.75	2.40	2.40						
DIP	25.32	6.33	4.79	4.80	4.80						
Leadless Carrier	N/A	N/A	8.54	10.00	N/A						
SWITCHES	6.96	N/A	N/A	N/A	1.20						
TRANSFORMERS	6.96	1.90	N/A	N/A	N/A	1	6.96				
RELAYS	13.18	3.57	N/A	N/A	2.40						
CONNECTORS (100 PIN)*											
Circular	187.0	59.9	50.1	30.0	N/A						
Printed Circuit	178.1	51.0	N/A	N/A	N/A	1 (25 PINS)		12.75			
Square Pin	179.7	33.6	25.2	30.0	30.0						
SHEET 2 SUMMATION							6.96	23.28			
SHEET 1 SUMMATION							11.76	18.60			
TOTAL SUMMATION							18.72	41.88			
PROCESS ALTERNATIVES							H	W	Vφ	IR	L

*Normalize for less than 100 pins.

5.3 Manufacturing Cost Data for Detail Design Phase

5.3.1 Mechanization Section

This section contains the format selection aid and formats for mechanization for electronic assemblies. Examples of the manufacturing cost data presented are for pin-outs, resistors, and interconnects. The formats presented in this section include cost-driver effects (CDE) and cost estimating data (CED).

5.3.1.1 Format Selection Aid

The format selection aid (Figure 5-6) indicates all the formats that can be utilized in the detail design process. Those related to mechanization are highlighted by the shaded box.

Some formats will be applicable at both the conceptual and detail design phases of electronic systems.

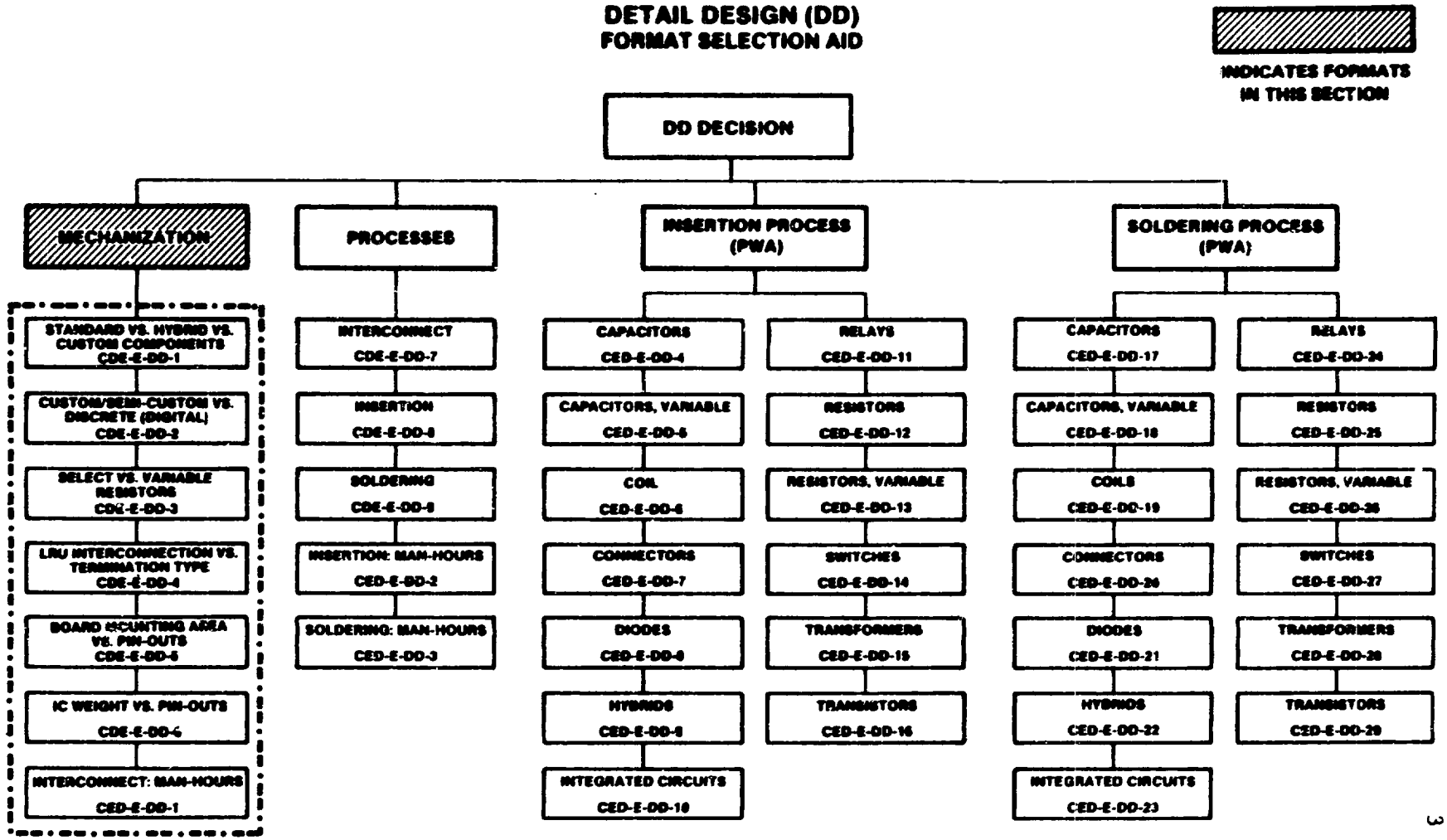


FIGURE 5-6. DETAIL DESIGN FORMAT SELECTION AID

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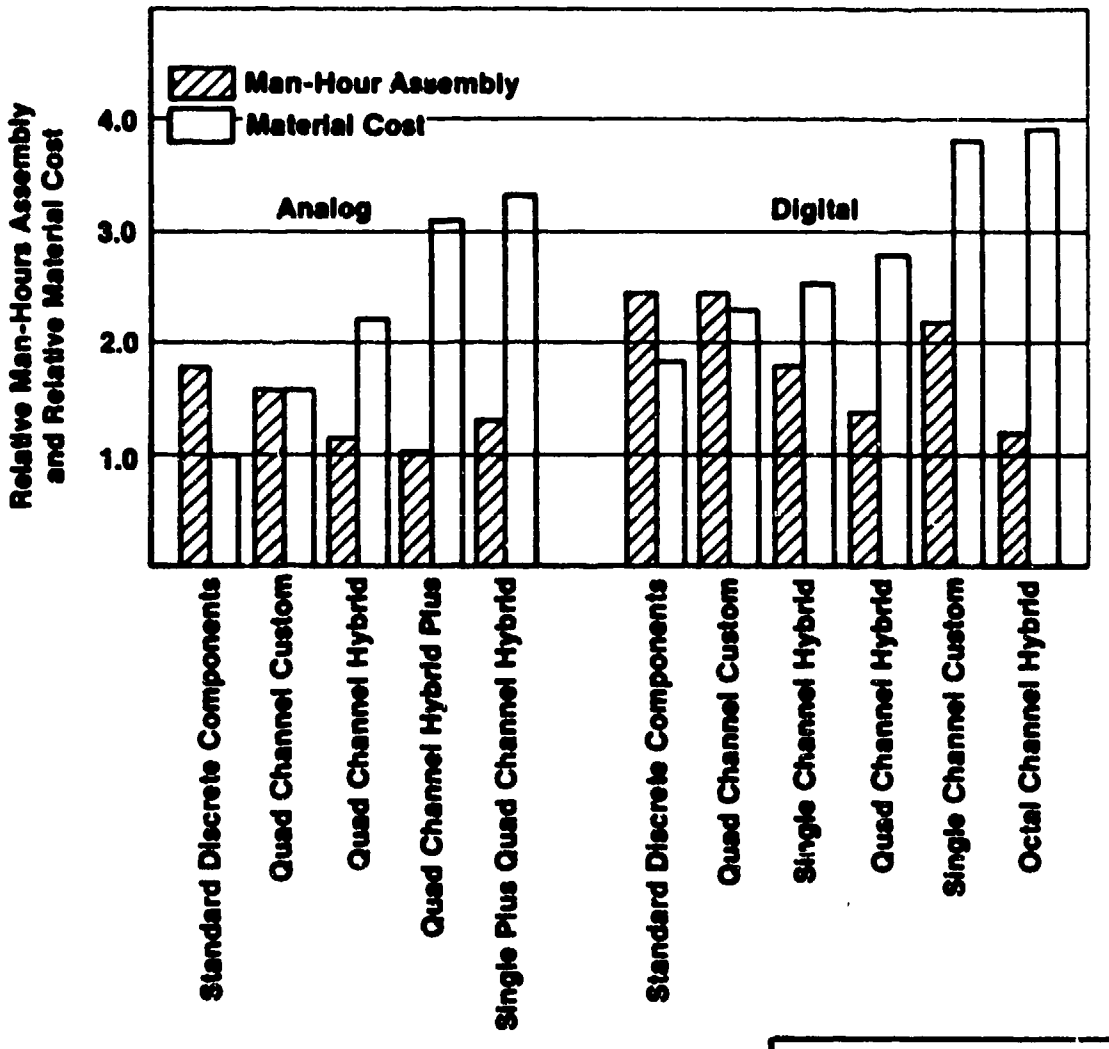
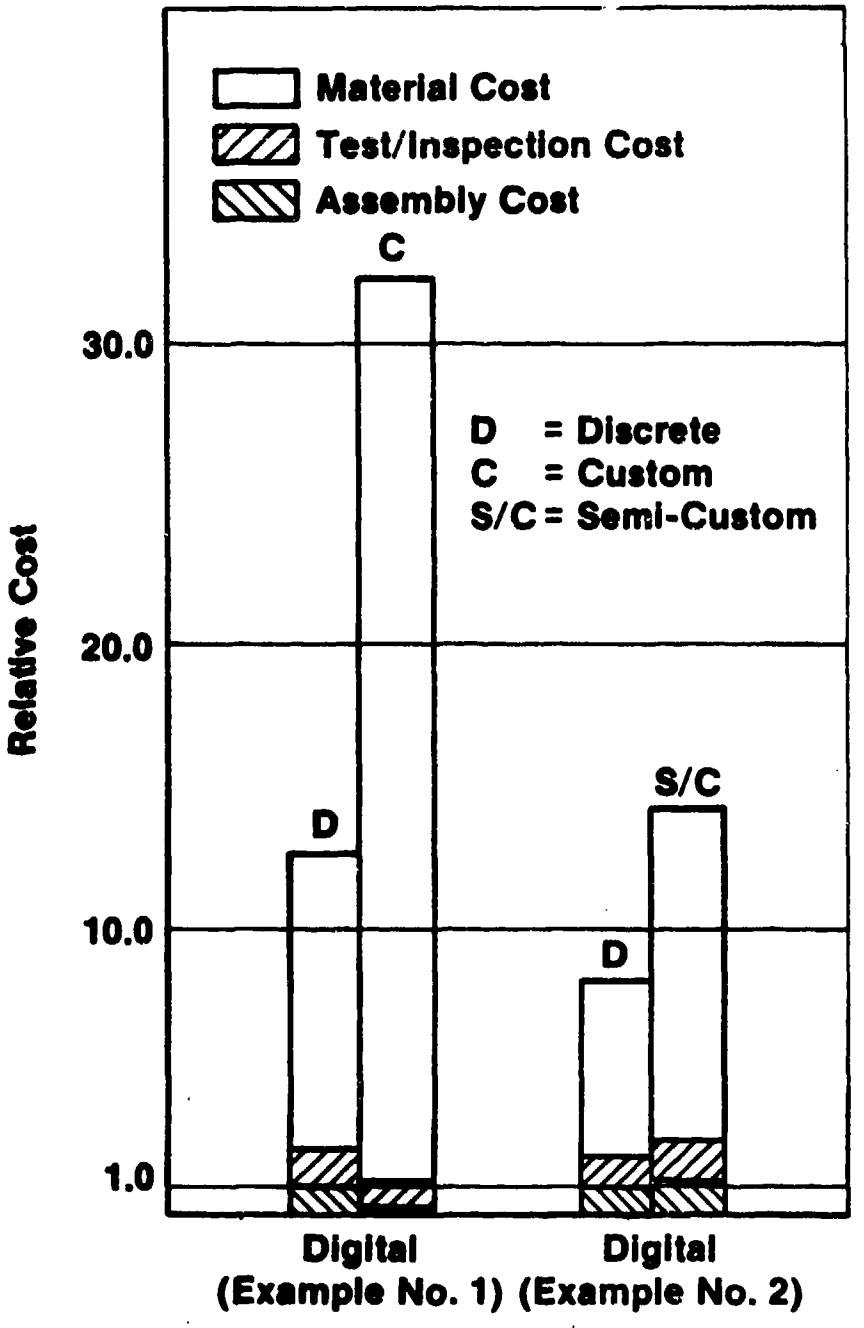
STANDARD DISCRETE VS. HYBRID AND CUSTOM



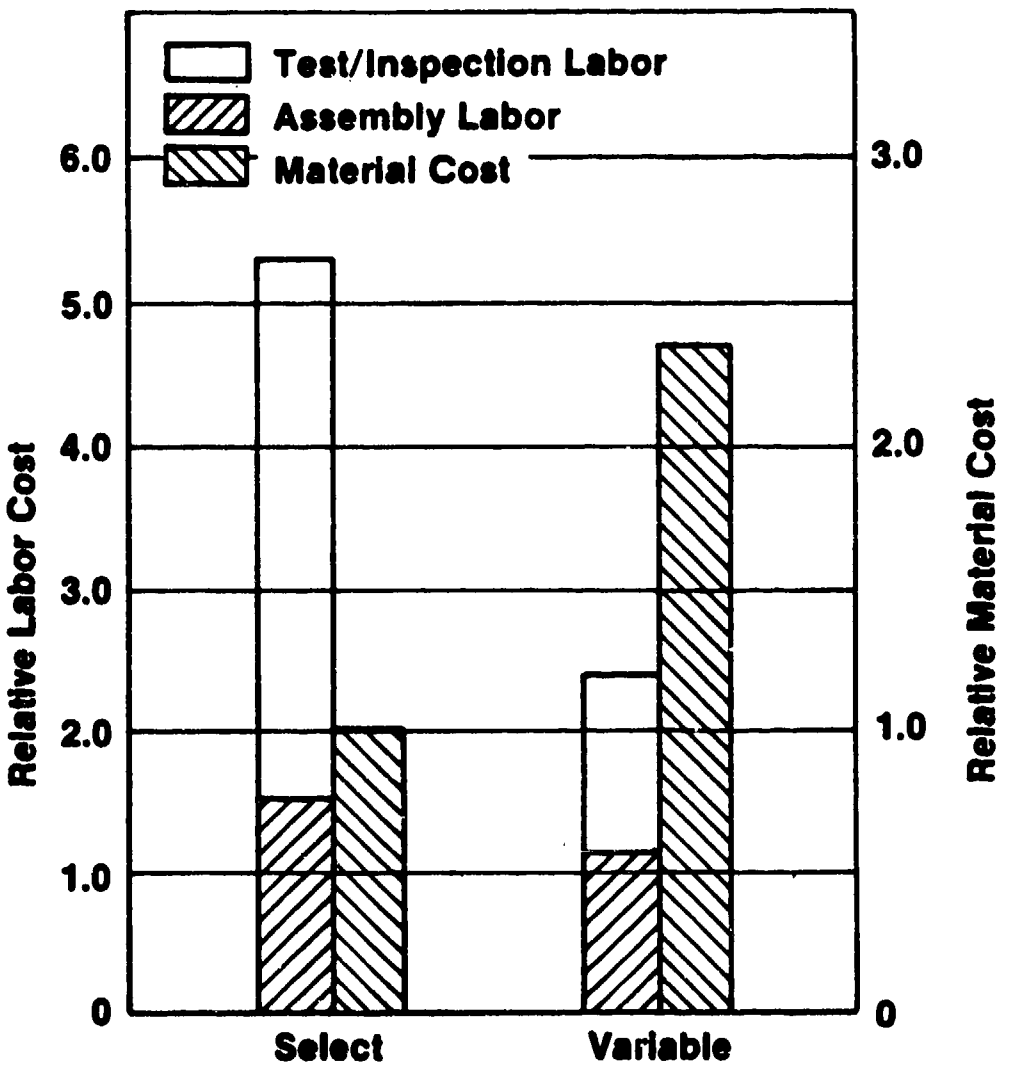
CDE-E-DD-1

CUSTOM/SEMI-CUSTOM VS. DISCRETE (DIGITAL)



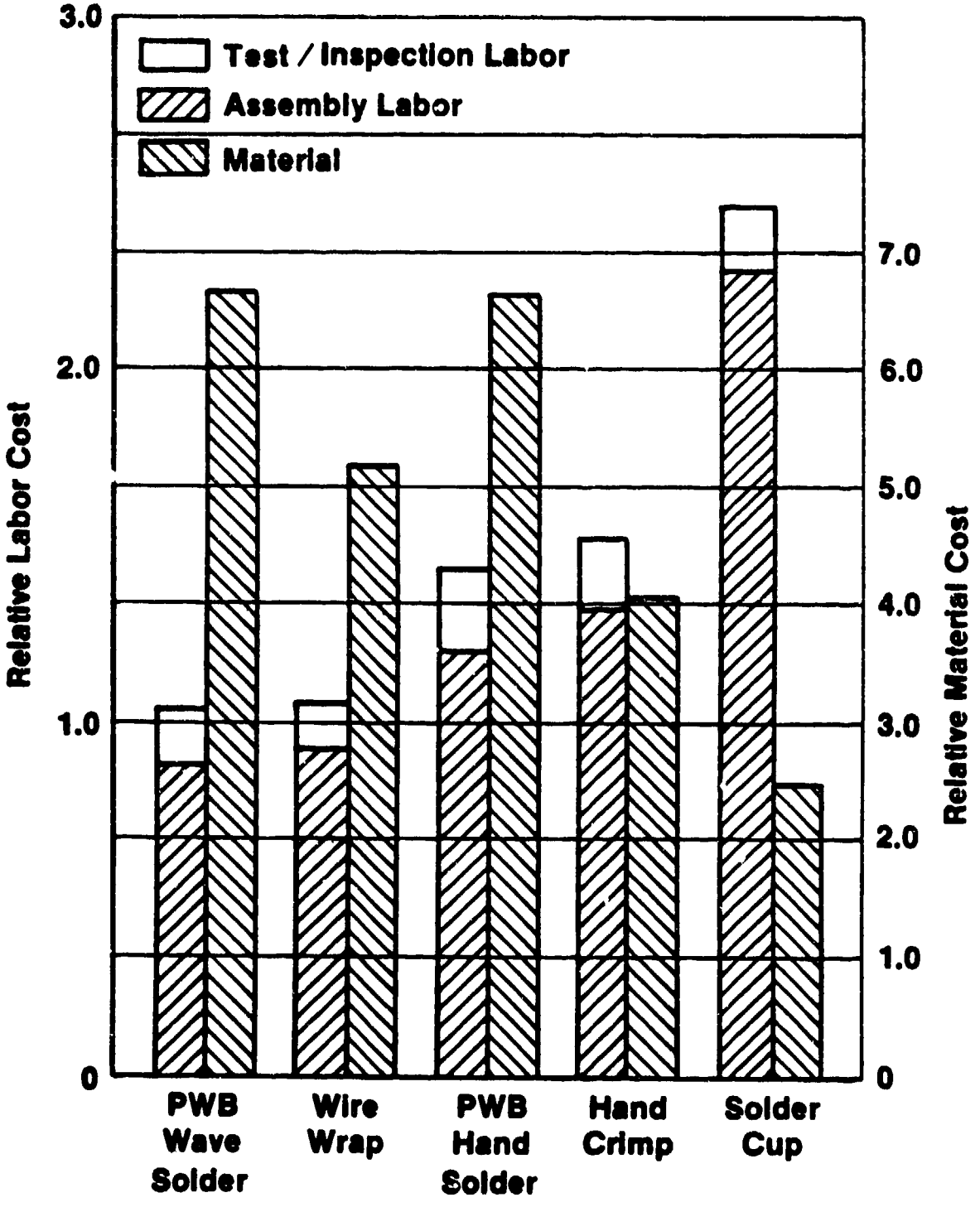
CDE-E-DD-2

MAN-HOURS/MATERIAL COST VS. RESISTOR TYPE



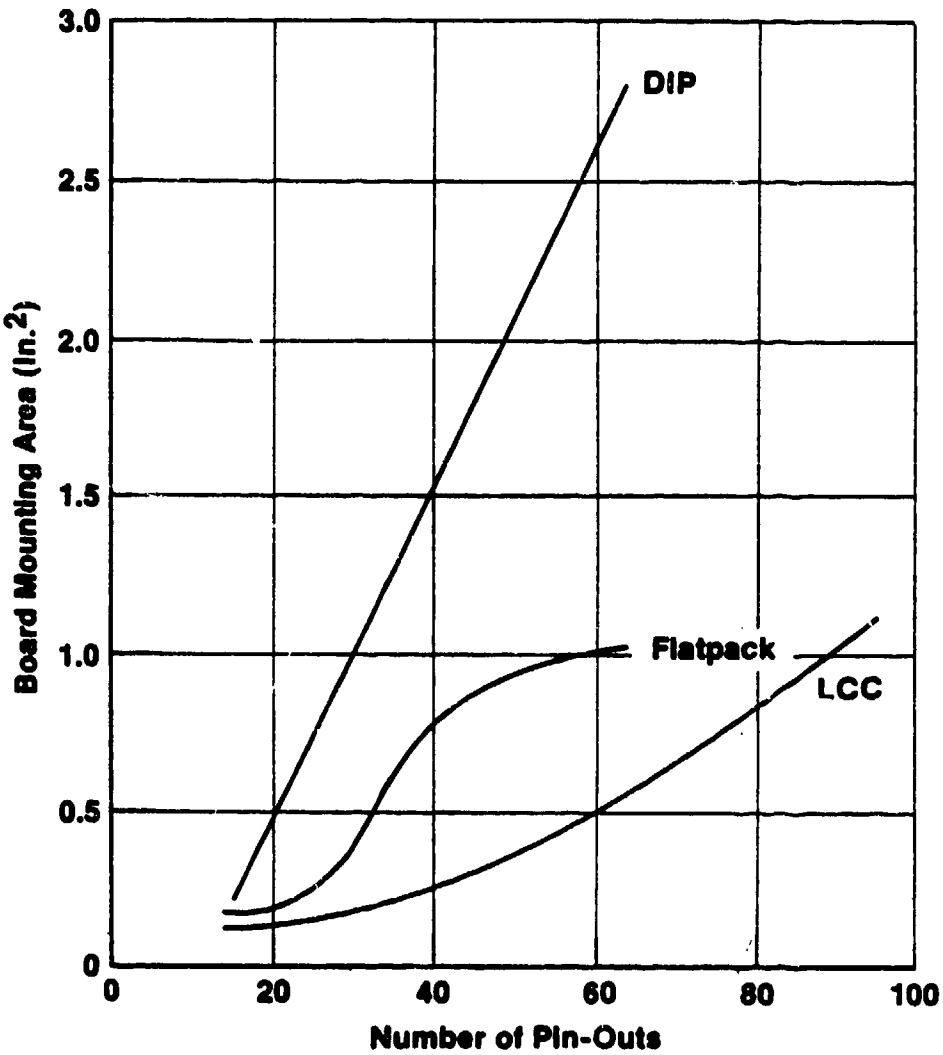
CDE-E-DD-3

LRU INTERCONNECTION MAN-HOURS AND MATERIAL COST VS. TERMINATION TYPE



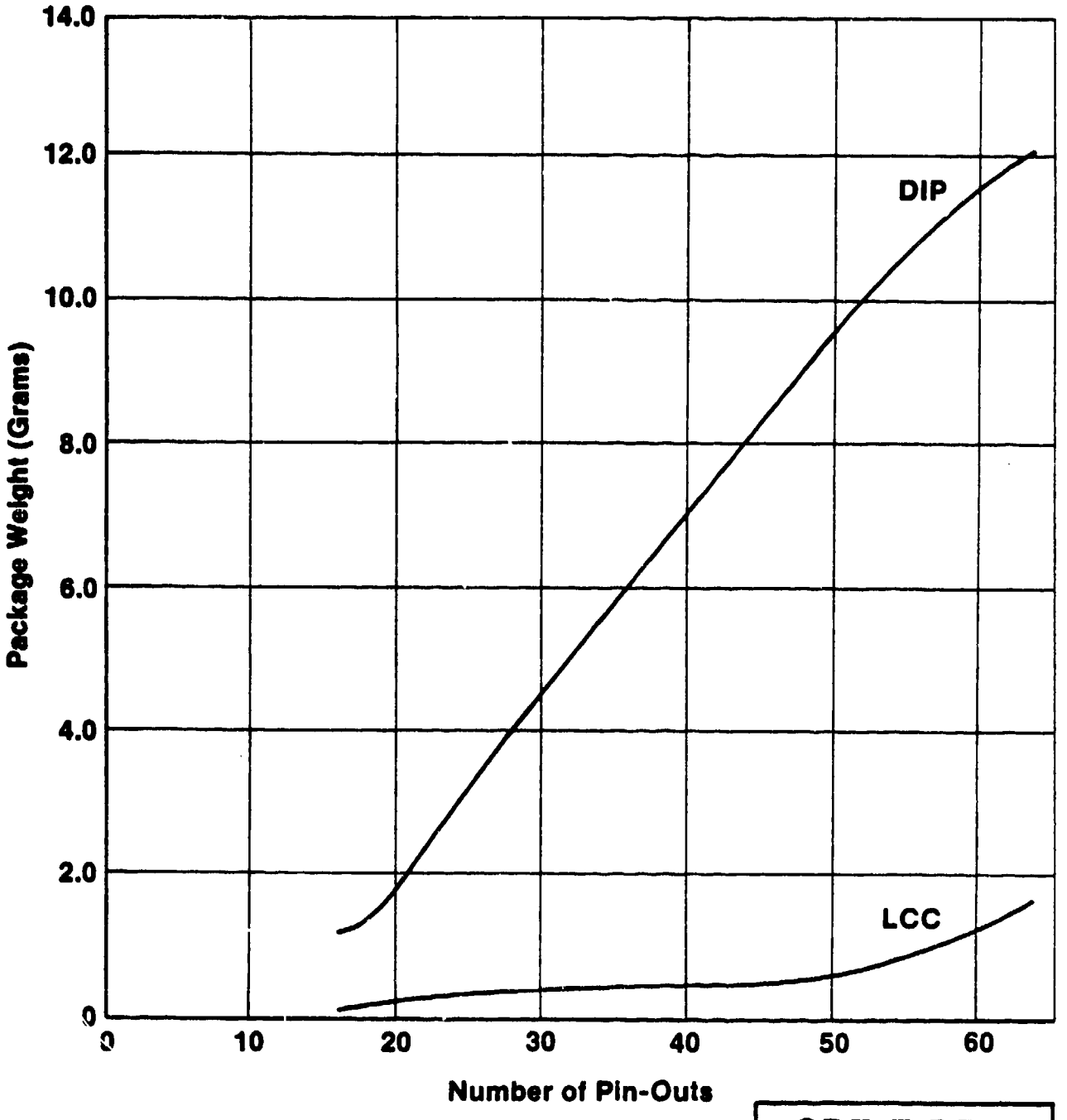
CDE-E-DD-4

BOARD MOUNTING AREA VS. NUMBER OF PIN-OUTS



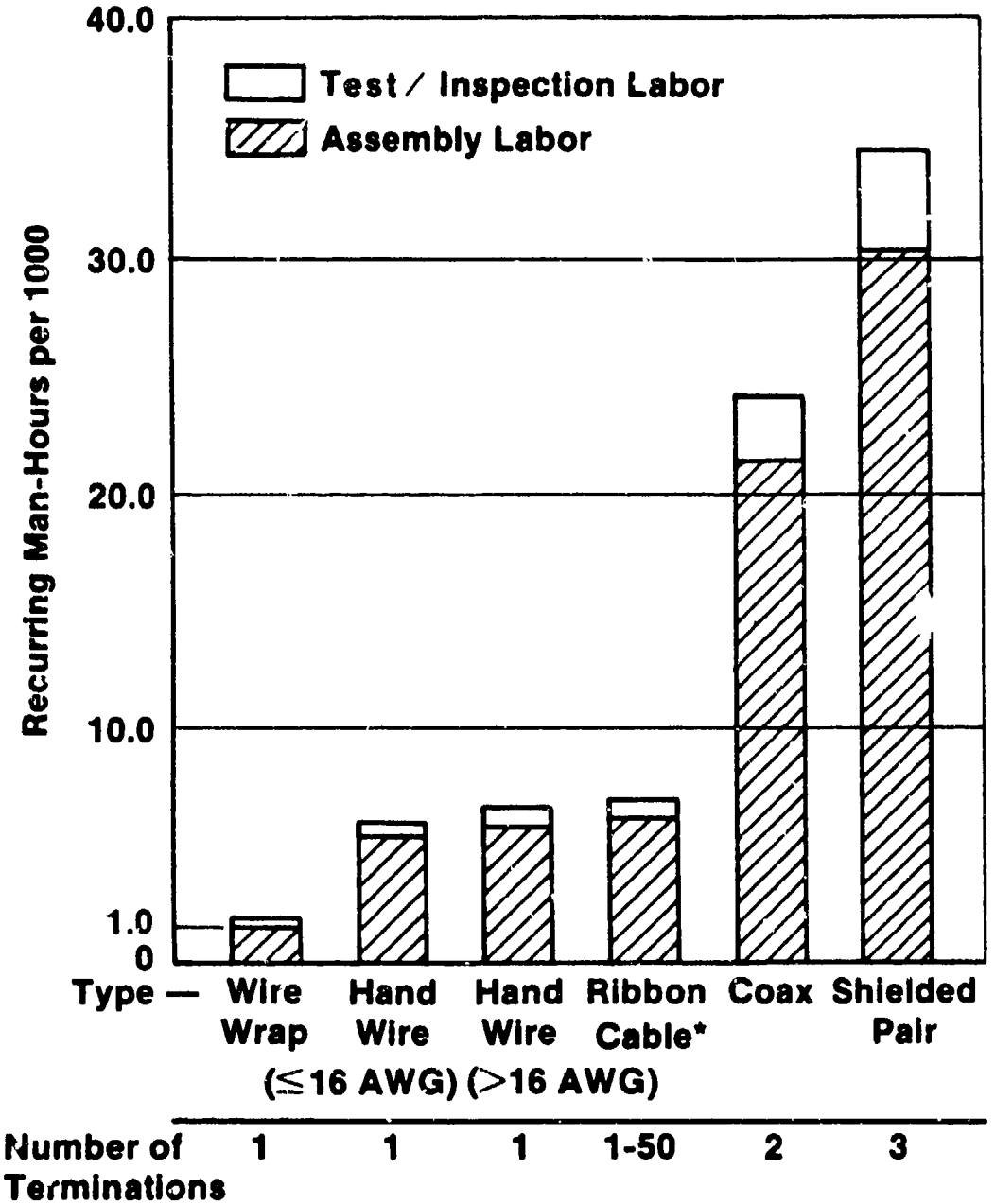
CDE-E-DD-5

I.C. PACKAGE WEIGHT VS. NUMBER OF PIN-OUTS



CDE-E-DD-6

INTERCONNECTIONS
MAN-HOURS PER TERMINATION TYPE



*Insulation Piercing Connector

CED-E-DD-1

5.3.2 Processes Section

This section contains the format selection aid and formats for both interconnect and soldering processes for electronic parts and assemblies. Example parts are resistors, capacitors, and diodes. Examples of assemblies are integrated circuits, hybrids, and transformers. The formats presented in this section include cost-driver effects (CDE) and cost estimating data (CED).

5.3.2.1 Format Selection Aid

The format selection aid (Figure 5-7) indicates all the formats that can be utilized in the detail design process. Those related to processes are highlighted by the shaded box.

Some formats will be applicable at both the conceptual and detail design phases of electronic systems.

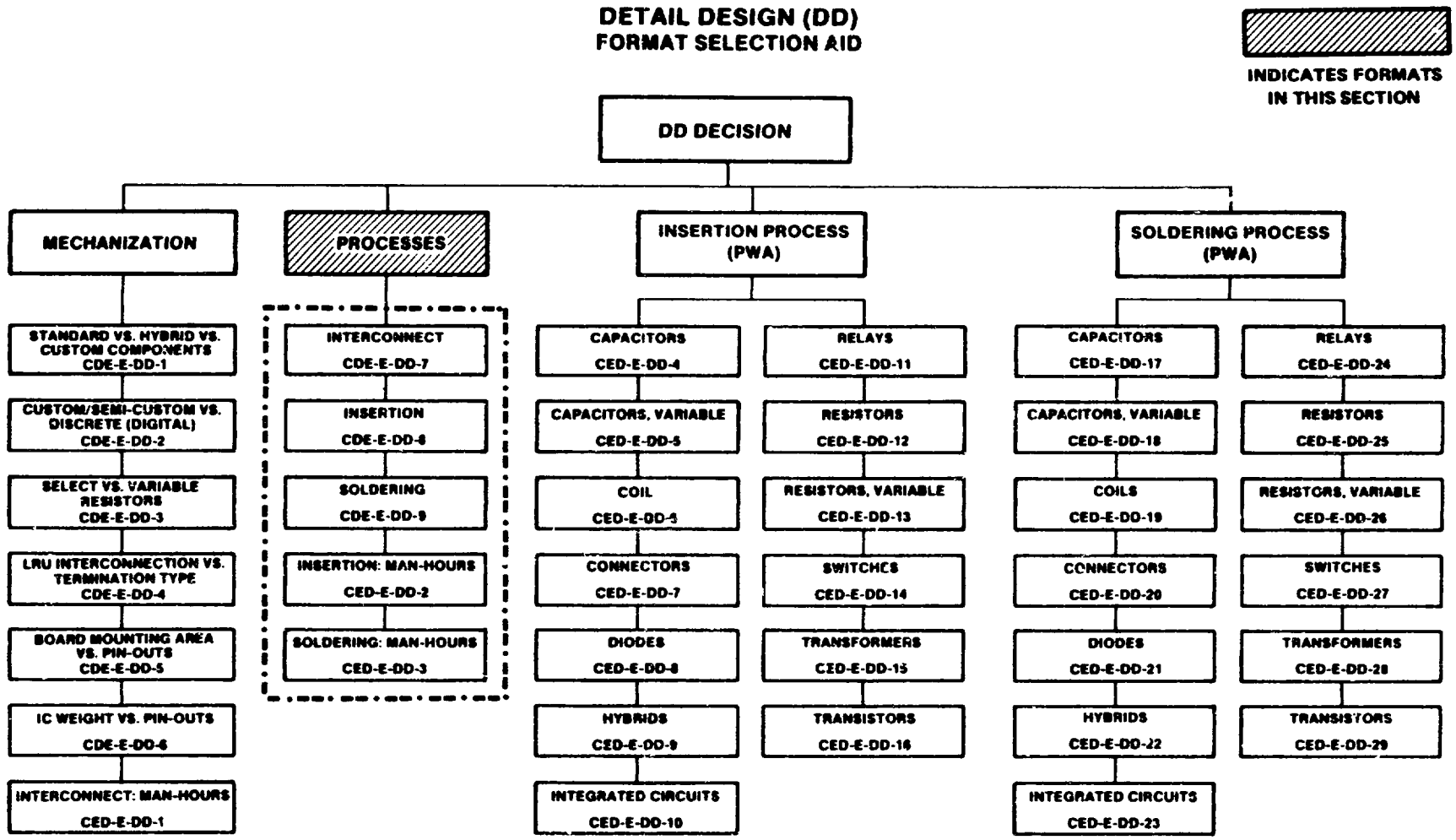


FIGURE 5-7. DETAIL DESIGN FORMAT SELECTION AID

FTR45026200OU
3 Jan 1983

PROCESS/MATERIAL CONSIDERATIONS FOR INTERCONNECT BETWEEN COMPONENTS

PROCESS	Polymide	G-10	Teflon	Ceramic	Multi-Wire
PART PACKAGE SUITABILITY					
Conventional Leaded	A	A	S	S	S
Beam Ribbon	S	A	S	A	N
Leadless	S	N	N	A	N
INSERTION/ATTACHMENT					
Hand	A	A	S	A	S
Semi-Auto	A	A	S	A	S
Auto	A	A	S	A	S
SOLDERING					
Hand	A	A	S	A	S
Wave	A	A	S	N	S
Vapor	S	S	S	A	S
Infrared	S	S	N	S	S
Laser	S	S	N	N	S

A Applicable

S Applicable (May Require Special Processing/Equipment)

N Not Applicable

CDE-E-DD-7

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

RELATIVE COST	LOW	MEDIUM	HIGH
INSERTION PROCESS	Auto	Semi-Auto	Hand
PART TYPE			
RESISTORS			
Axial Leaded	A	A	A
DIP	S	A	A
SIP	N	A	A
Chip	A	S	A
VARIABLE RESISTORS			
Sealed	N	A	A
Open	N	A	A
CAPACITORS			
Axial Leaded	A	A	A
Radial Leaded	A	A	A
DIP	A	A	A
SIP	N	A	A
Chip	A	S	A
VARIABLE CAPACITORS			
Opened	N	A	A
Sealed	N	A	A
COILS			
Axial Leaded	S	A	A
Variable	N	N	S
DIODES	A	A	A
TRANSISTORS			
Standard Leaded	N	A	A
Ribbon Leaded	N	N	A

A Applicable

S Applicable (May Require Special Processing/Equipment)

N Not Applicable

CDE-E-DD-8

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED) (CONTINUED)

RELATIVE COST	LOW	MEDIUM	HIGH
INSERTION PROCESS	Auto	Semi-Auto	Hand
PART TYPE			
INTEGRATED CIRCUITS			
Flatpacks	N	S	A
Canned	N	A	A
DIP	S	A	A
Leadless Carrier (28 Pin-Out)	A	S	A
MIP (100 Pin-Out)	N	A	A
HYBRIDS			
Flatpacks	N	S	A
Canned	N	A	A
DIP	A	A	A
MIP (28 Pin-Out)	N	A	A
SWITCHES	N	N	A
TRANSFORMERS	N	N	A
RELAYS	N	N	A
CONNECTORS			
Circular	N	N	A
Printed Circuit	N	N	A
Square Pin	A	A	A

A Applicable

S Applicable (May Require Special Processing/Equipment)

N Not Applicable

CDE-E-DD-8

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)

RELATIVE COST	LOW	LOW	MEDIUM	MEDIUM	HIGH
SOLDERING PROCESS	Infrared*	Laser*	Wave	Vapor Phase*	Hand
PART TYPE					
RESISTORS					
Axial Leaded	A	A	A	A	A
DIP	A	A	A	A	A
SIP	A	A	A	A	A
Chip	A	N	A	A	S
VARIABLE RESISTORS					
Sealed	A	A	A	A	A
Open	A	S	N	N	A
CAPACITORS					
Axial Leaded	A	A	A	A	A
Radial Leaded	A	A	A	A	A
DIP	A	A	A	A	A
SIP	A	A	A	A	A
Chip	A	N	A	A	S
VARIABLE CAPACITORS					
Sealed	A	A	A	A	A
Open	S	N	N	N	A
COILS					
Axial Leaded	A	A	A	A	A
Variable	S	N	A	A	S
DIODES	N	N	A	A	A
TRANSISTORS					
Standard Leaded	A	A	A	A	A
Ribbon Leaded	A	N	N	A	A

*Pre-Applied Solder/Flux Required

A Applicable

S Applicable (May Require Special Processing/Equipment)

N Not Applicable

CDE-E-DD-9

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED) (CONTINUED)

RELATIVE COST	LOW	LOW	MEDIUM	MEDIUM	HIGH
SOLDERING PROCESS	Infrared*	Laser*	Wave	Vapor Phase*	Hand
PART TYPE					
INTEGRATED CIRCUITS					
Flatpacks	A	A	S	A	A
Canned	A	A	A	A	A
DIP	A	A	A	A	A
Leadless Carrier (28 Pin-Out)	A	N	N	A	N
MIP (100 Pin-Out)	A	N	A	A	A
HYBRIDS					
Flatpacks	A	A	S	A	A
Canned	A	A	A	A	A
DIP	A	A	A	A	A
Leadless Carrier (28 Pin-Out)	A	N	N	A	N
MIP (100 Pin-Out)	A	N	A	A	A
SWITCHES	N	A	N	N	A
TRANSFORMERS	N	N	S	N	A
RELAYS	N	S	S	N	A
CONNECTORS					
Circular	S	N	S	S	A
Printed Circuit	N	N	A	N	A
Square Pin	A	A	S	A	A

*Pre-Applied Solder/Flux Required

A Applicable

S Applicable (May Require Special Processing/Equipment)

N Not Applicable

CDE-E-DD-9

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED) MAN-HOURS PER 1000

RELATIVE COST	LOW	MEDIUM	HIGH
INSERTION PROCESS	Auto	Semi-Auto	Hand
PART TYPE			
RESISTORS			
Axial Leaded	0.29	2.39	2.94
DIP	0.44	4.44	4.74
SIP	N/A	3.00	3.34
Chip	0.47	1.20	2.10
VARIABLE RESISTORS			
Sealed	N/A	4.00	4.59
Open	N/A	4.00	4.59
CAPACITORS			
Axial Leaded	0.29	2.39	2.94
Radial Leaded	0.29	2.89	3.14
DIP	0.44	4.40	4.74
SIP	N/A	3.00	3.34
Chip	0.47	1.20	2.10
VARIABLE CAPACITORS			
Opened	N/A	2.34	2.59
Sealed	N/A	2.34	2.59
COILS			
Axial Leaded	0.25	2.39	2.94
Variable	N/A	N/A	2.50
DIODES	0.25	1.83	2.33
TRANSISTORS			
Standard Leaded	N/A	3.74	4.20
Ribbon Leaded	N/A	N/A	7.83

CED-E-DD-2

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED) MAN-HOURS PER 1000 (CONTINUED)

RELATIVE COST	LOW	MEDIUM	HIGH
INSERTION PROCESS	Auto	Semi-Auto	Hand
PART TYPE			
INTEGRATED CIRCUITS			
Flatpacks	N/A	5.80	4.32
Canned	N/A	6.95	7.84
DIP	0.44	4.40	4.74
Leadless Carrier (28 Pin-Out)	0.55	8.00	7.67
MIP (100 Pin-Out)	N/A	3.00	3.34
HYBRIDS			
Flatpacks	N/A	5.80	4.32
Canned	N/A	6.95	7.84
DIP	0.44	4.40	4.74
MIP (100 Pin-Out)	N/A	3.00	3.34
SWITCHES	N/A	N/A	4.37
TRANSFORMERS	N/A	N/A	5.17
RELAYS	N/A	N/A	5.04
CONNECTORS			
Circular	N/A	N/A	118.35
Printed Circuit	N/A	N/A	79.75
Square Pin	13.33	60.00	86.65

CED-E-DD-2

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED) MAN-HOURS PER 1000

RELATIVE COST	LOW	LOW	MEDIUM	MEDIUM	HIGH
SOLDERING PROCESS	Infrared*	Laser*	Wave	Vapor Phase*	Hand
PART TYPE					
RESISTORS					
Axial Leaded	0.60	0.60	0.84	0.64	3.90
DIP	4.80	4.80	6.33	4.79	25.32
SIP	2.40	2.40	3.57	2.75	13.18
Chip	0.60	N/A	0.60	0.65	15.54
VARIABLE RESISTORS					
Sealed	0.90	0.90	1.88	1.57	5.88
Open	0.90	0.90	N/A	N/A	5.88
CAPACITORS					
Axial Leaded	0.60	0.60	0.84	0.64	3.90
Radial Leaded	0.60	0.60	0.84	0.64	3.90
DIP	4.80	4.80	6.33	4.79	25.32
SIP	2.40	2.40	3.57	2.75	13.18
Chip	0.60	N/A	0.60	0.65	15.54
VARIABLE CAPACITORS					
Sealed	0.90	0.90	1.88	1.57	4.70
Open	0.90	N/A	N/A	N/A	4.60
COILS					
Axial Leaded	0.60	0.60	0.84	0.64	3.90
Variable	0.60	N/A	1.60	1.19	4.67
DIODES	N/A	N/A	1.08	0.67	4.60
TRANSISTORS					
Standard Leaded	0.90	0.90	1.40	1.09	5.40
Ribbon Leaded	1.30	N/A	N/A	2.62	7.71

*Pre-Applied Solder/Flux Required

CED-E-DD-3

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED) MAN-HOURS PER 1000 (CONTINUED)

RELATIVE COST	LOW	LOW	MEDIUM	MEDIUM	HIGH
SOLDERING PROCESS	Infrared*	Laser*	Wave	Vapor Phase*	Hand
PART TYPE					
INTEGRATED CIRCUITS					
Flatpacks	4.20	4.20	4.20	4.20	25.67
Canned	2.40	2.40	3.57	2.75	13.18
DIP	4.80	4.80	6.33	4.79	25.32
Leadless Carrier (28 Pin-Out)	10.00	N/A	N/A	8.54	N/A
MIP (100 Pin-Out)	30.00	N/A	30.00	30.00	160.00
HYBRIDS					
Flatpacks	4.20	4.20	4.20	4.20	25.67
Canned	2.40	2.40	3.57	2.75	13.18
DIP	4.80	4.80	6.33	4.79	25.32
Leadless Carrier (28 Pin-Out)	10.00	N/A	N/A	8.54	N/A
MIP (100 Pin-Out)	30.00	N/A	30.00	30.00	160.00
SWITCHES	N/A	1.20	N/A	N/A	6.96
TRANSFORMERS	N/A	N/A	1.90	N/A	6.96
RELAYS	N/A	2.40	3.57	N/A	13.18
CONNECTORS					
Circular	30.00	N/A	59.92	50.08	186.95
Printed Circuit	N/A	N/A	51.04	N/A	178.05
Square Pin	30.00	30.00	33.57	25.15	179.65

*Pre-Applied Solder/Flux Required

CED-E-DD-3

5.3.3 Insertion Process Section

This section contains the format selection aid and formats for the insertion process of printed wiring assemblies (PWA). Examples of assemblies are coils, integrated circuits, and switches. The formats presented in this section include cost-driver effects (CDE) and cost estimating data (CED).

5.3.3.1 Format Selection Aid

The format selection aid (Figure 5-8) indicates all the formats that can be utilized in the detail design process. Those related to the insertion processes are highlighted by the shaded box.

Some formats will be applicable at both the conceptual and detail design phases of electronic systems.

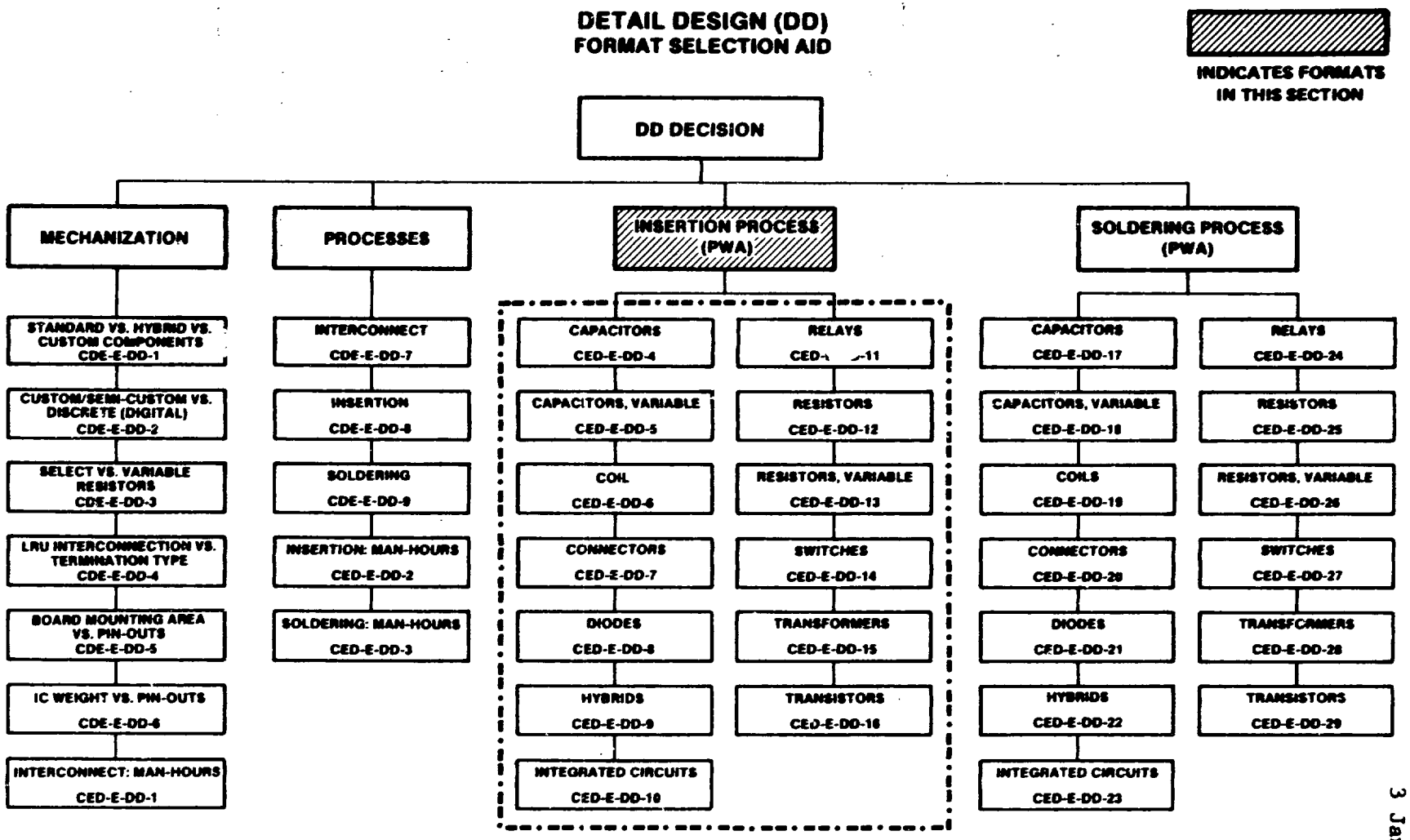
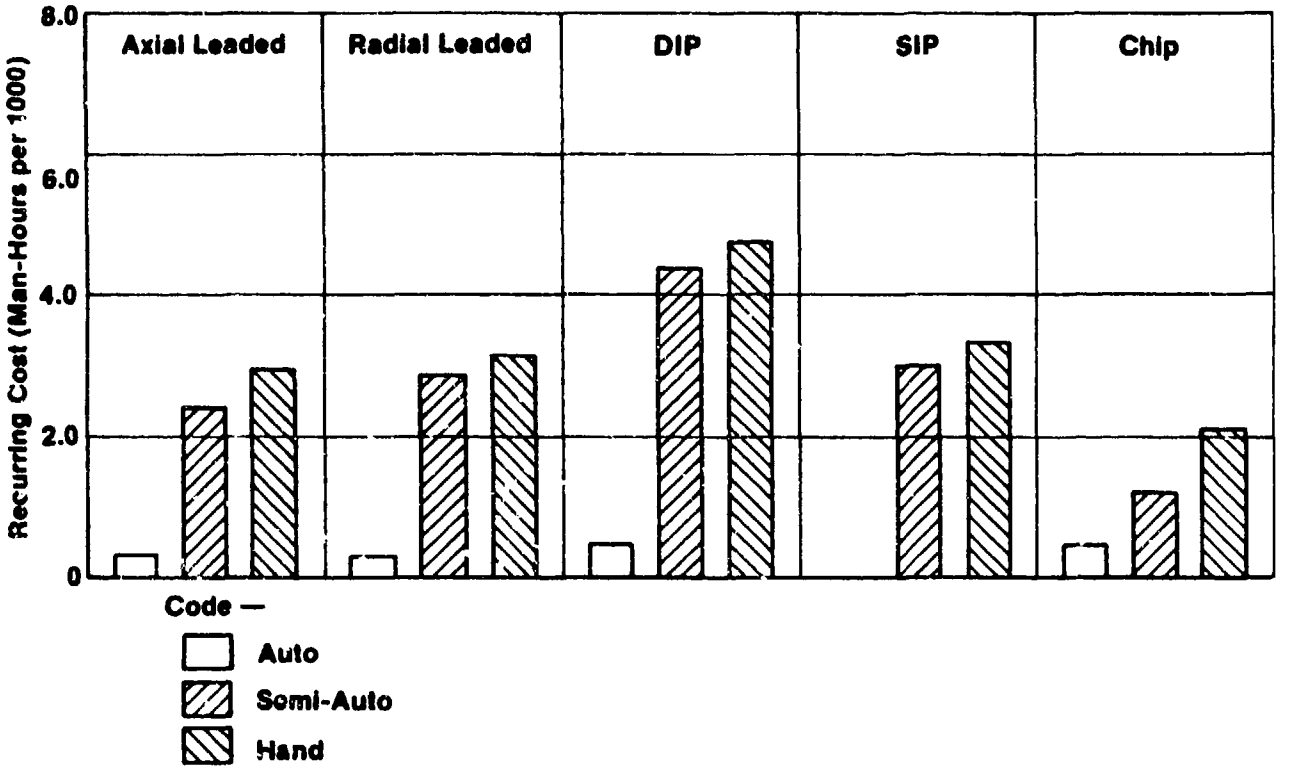


FIGURE 5-8. DETAIL DESIGN FORMAT SELECTION AID

FTR45026200OU
3 Jan 1983

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

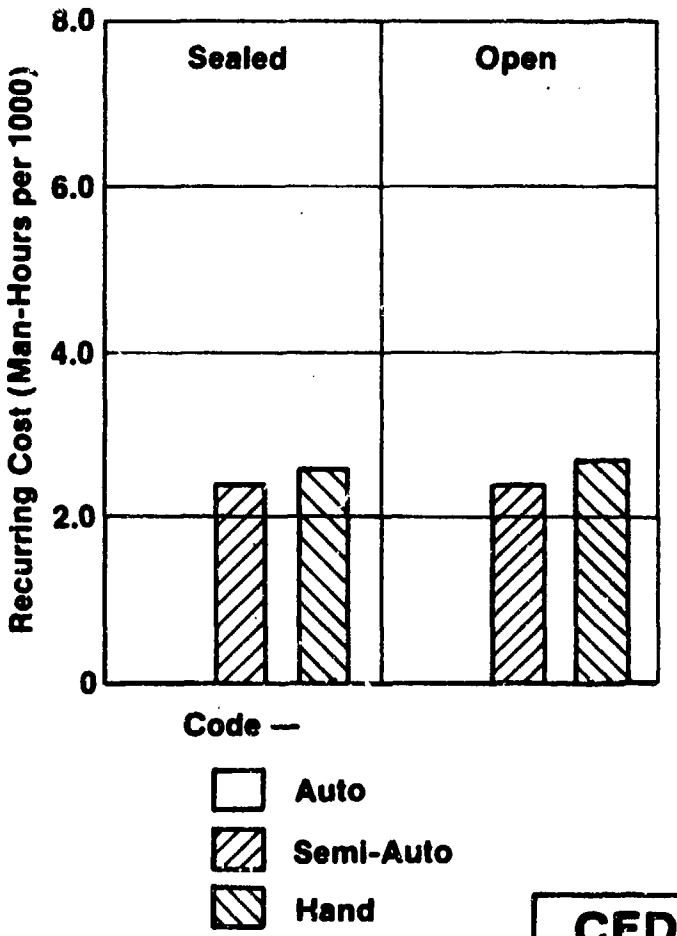
CAPACITORS



CED-E-DD-4

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

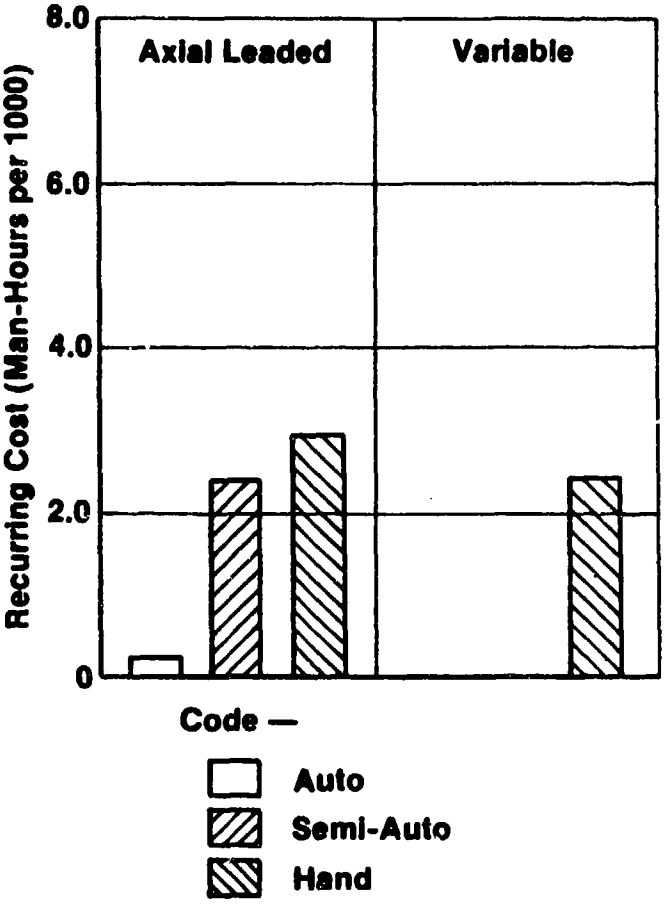
CAPACITORS,VARIABLE



CED-E-DD-5

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

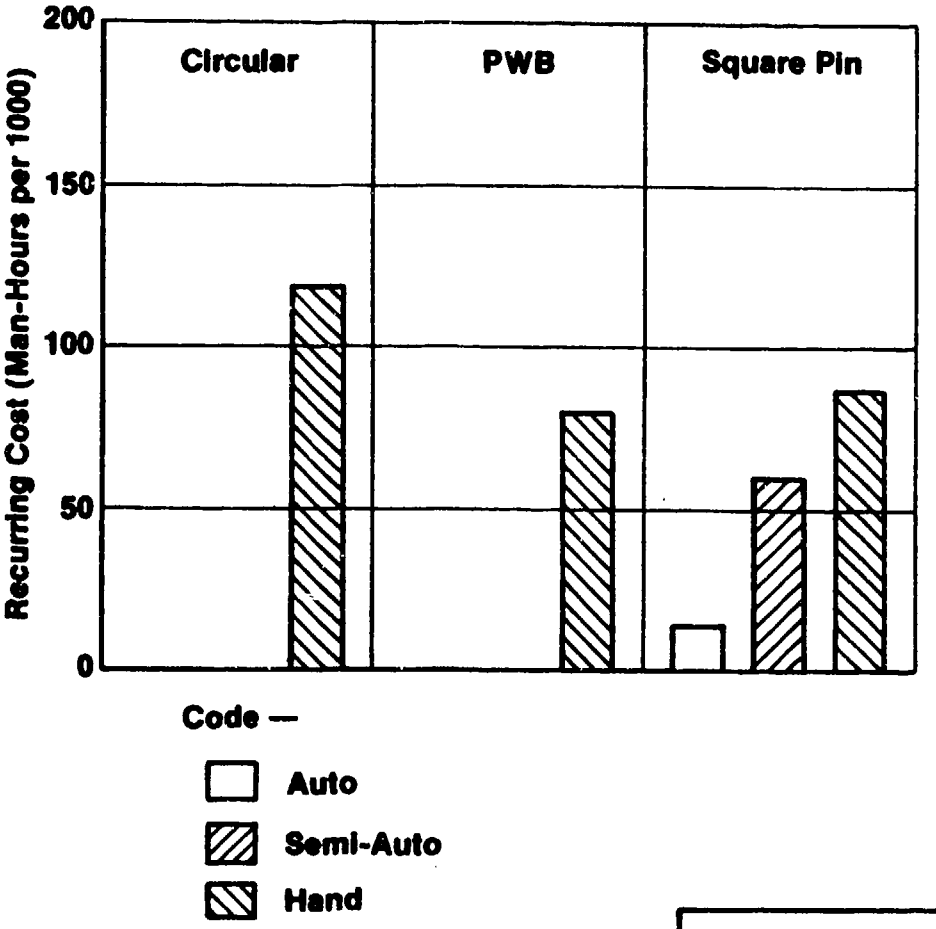
COIL



CED-E-DD-6

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

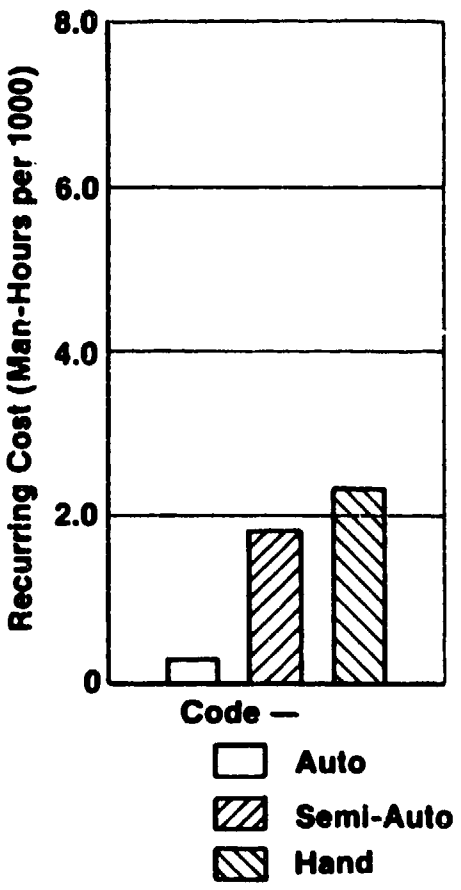
CONNECTORS



CED-E-DD-7

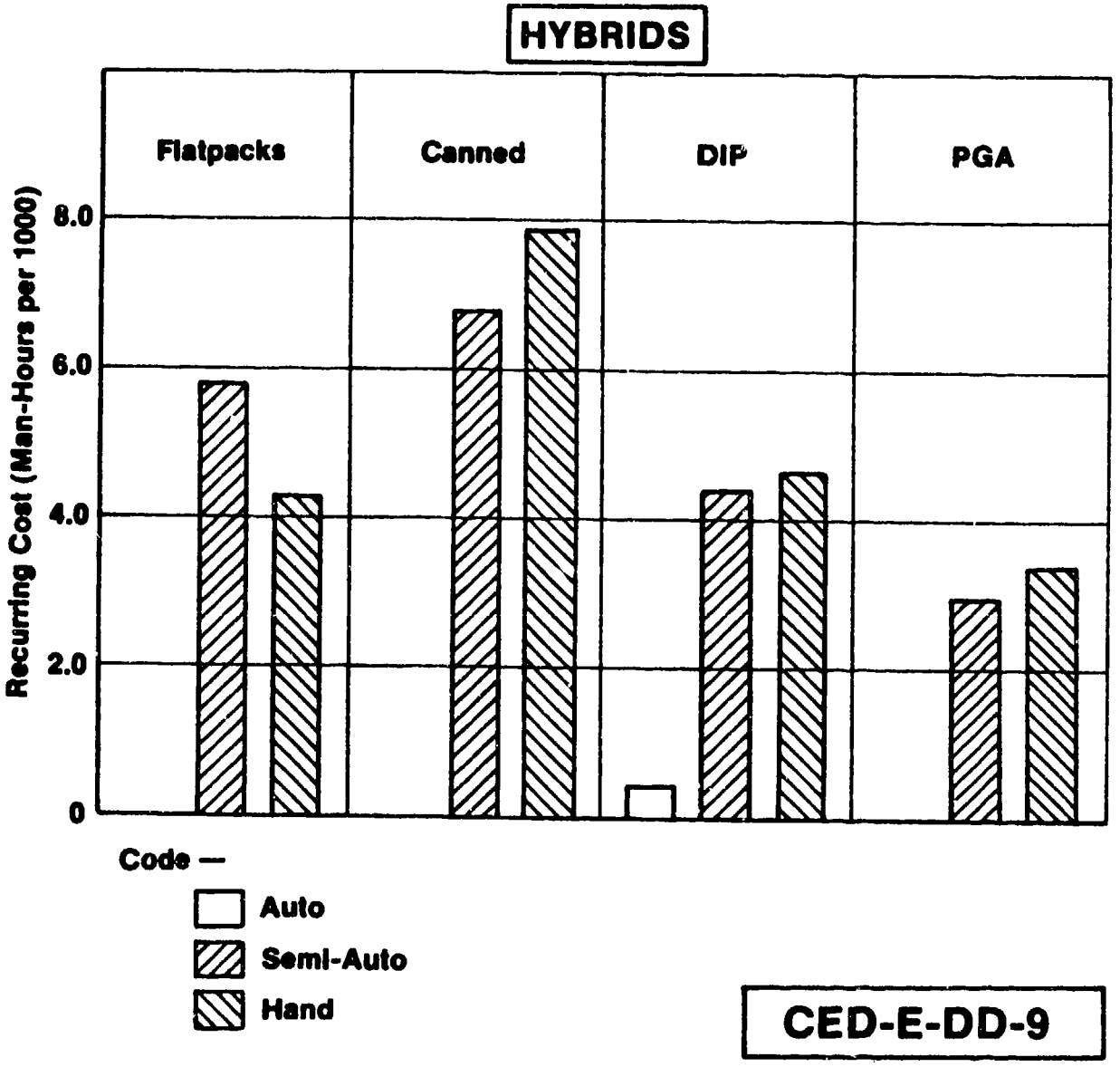
INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

DIODES



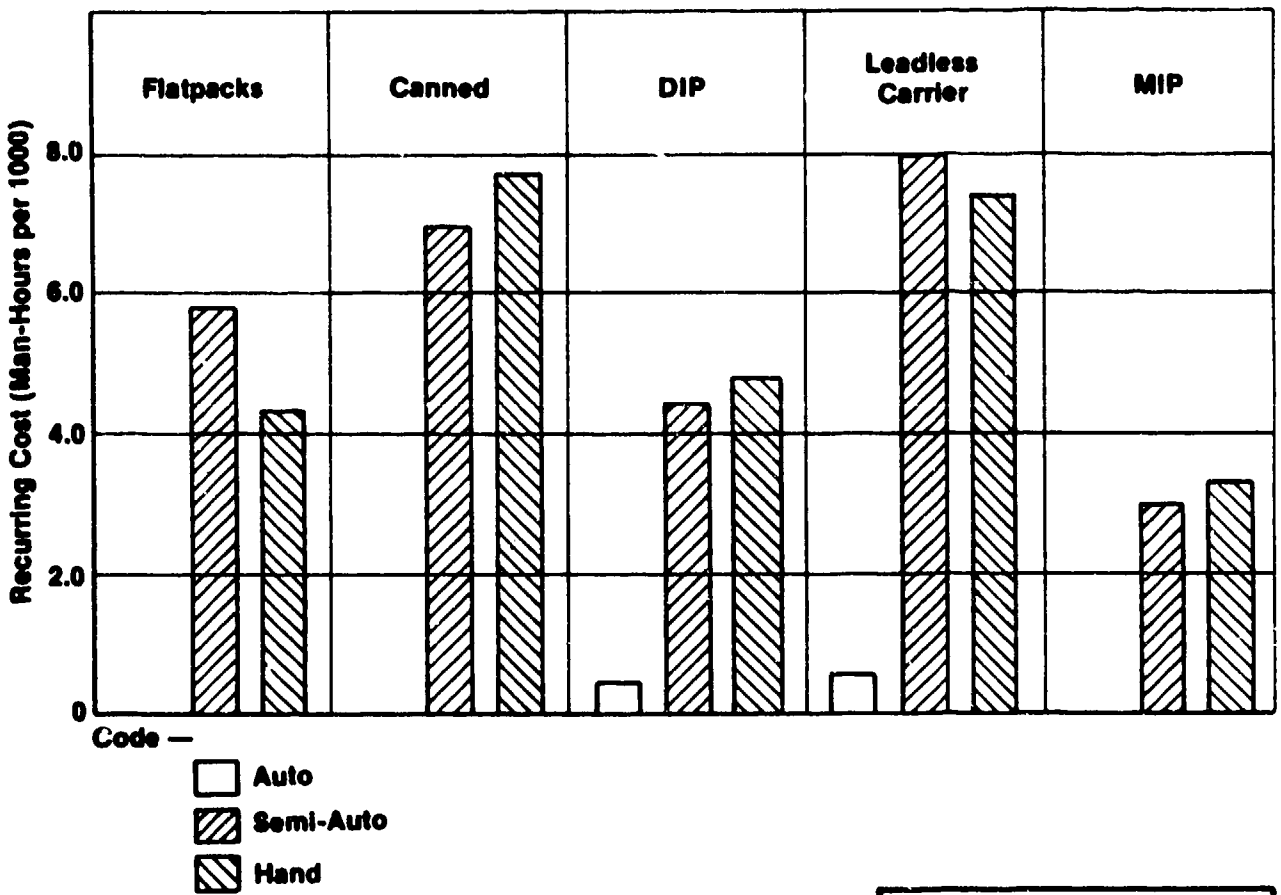
CED-E-DD-8

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)



INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

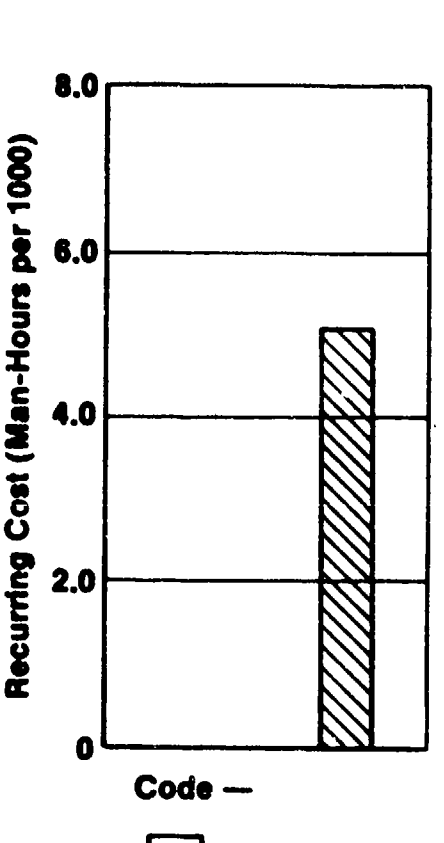
INTEGRATED CIRCUITS



CED-E-DD-10

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

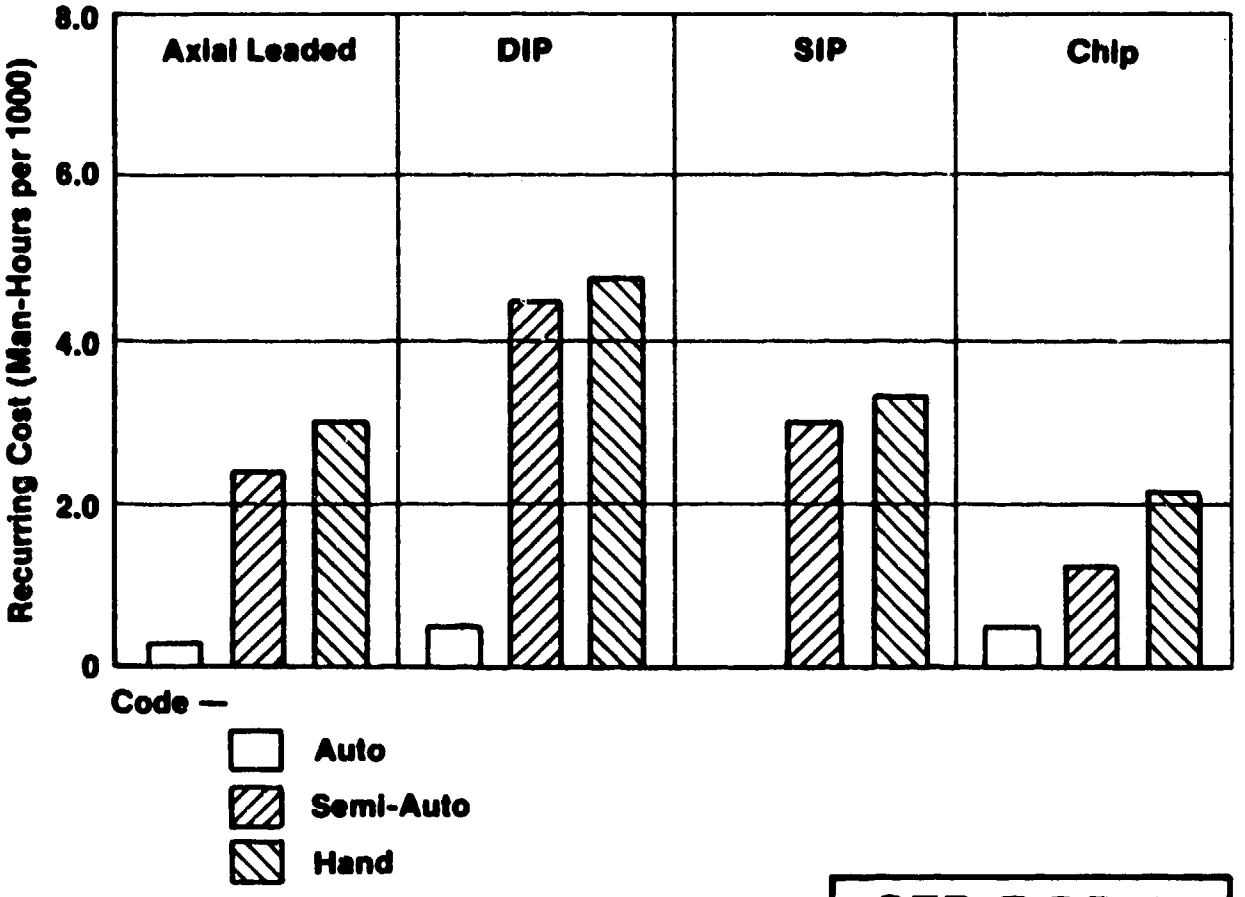
RELAYS



CED-E-DD-11

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

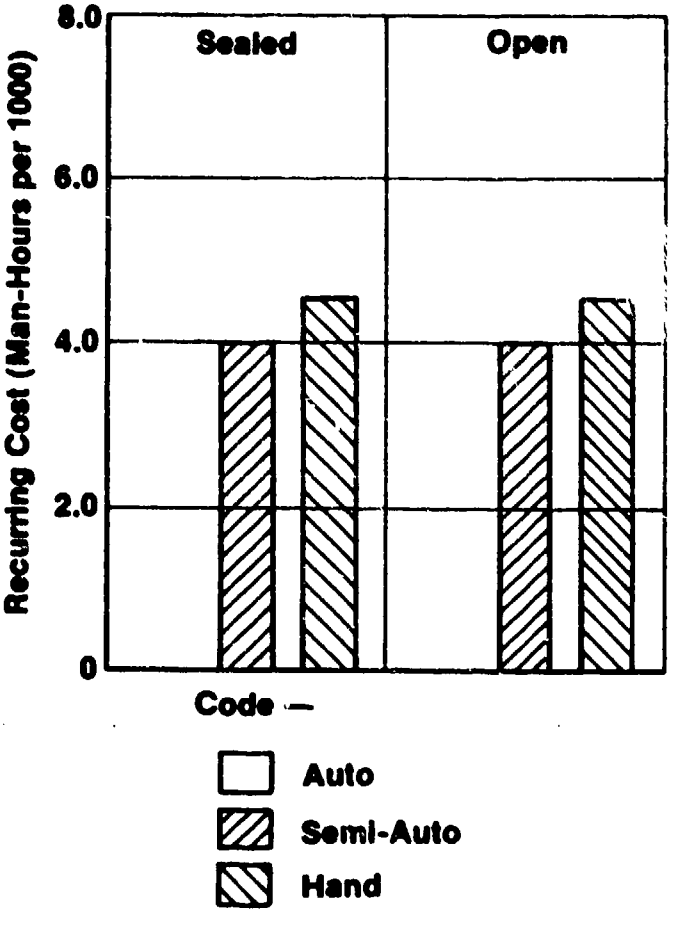
RESISTORS



CED-E-DD-12

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

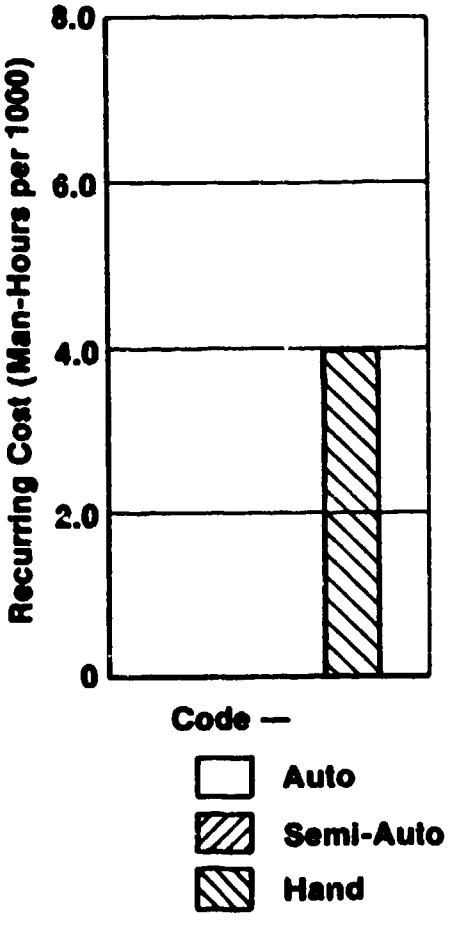
RESISTORS, VARIABLE



CED-E-DD-13

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

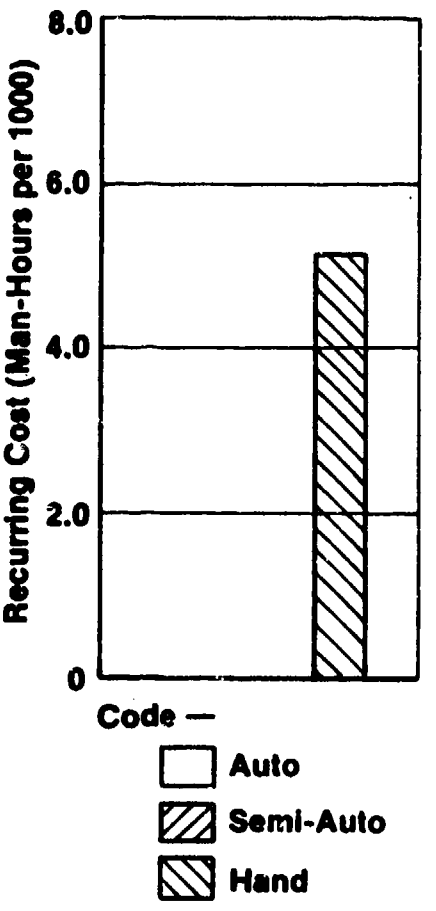
SWITCHES



CED-E-DD-14

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

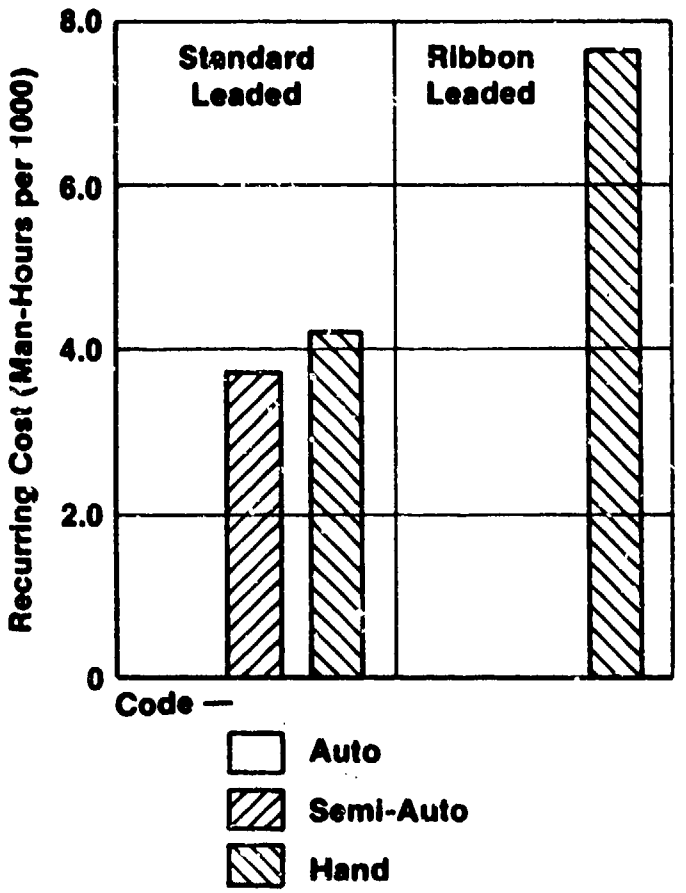
TRANSFORMERS



CED-E-DD-15

INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

TRANSISTORS



CED-E-DD-16

5.3.4 Soldering Process Section

This section contains the format selection aid and formats for the soldering process applied to printed wiring assemblies (PWA). Example parts are capacitors, coils, diodes, and transistors. The formats presented in this section include cost-driver effects (CDE) and cost estimating data (CED).

5.3.4.1 Format Selection Aid

The format selection aid (Figure 5-9) indicates all the formats that can be utilized in the detail design process. Those related to the soldering process (PWA) are highlighted by the shaded box.

Some formats will be applicable at both the conceptual and detail design phases of electronic systems.

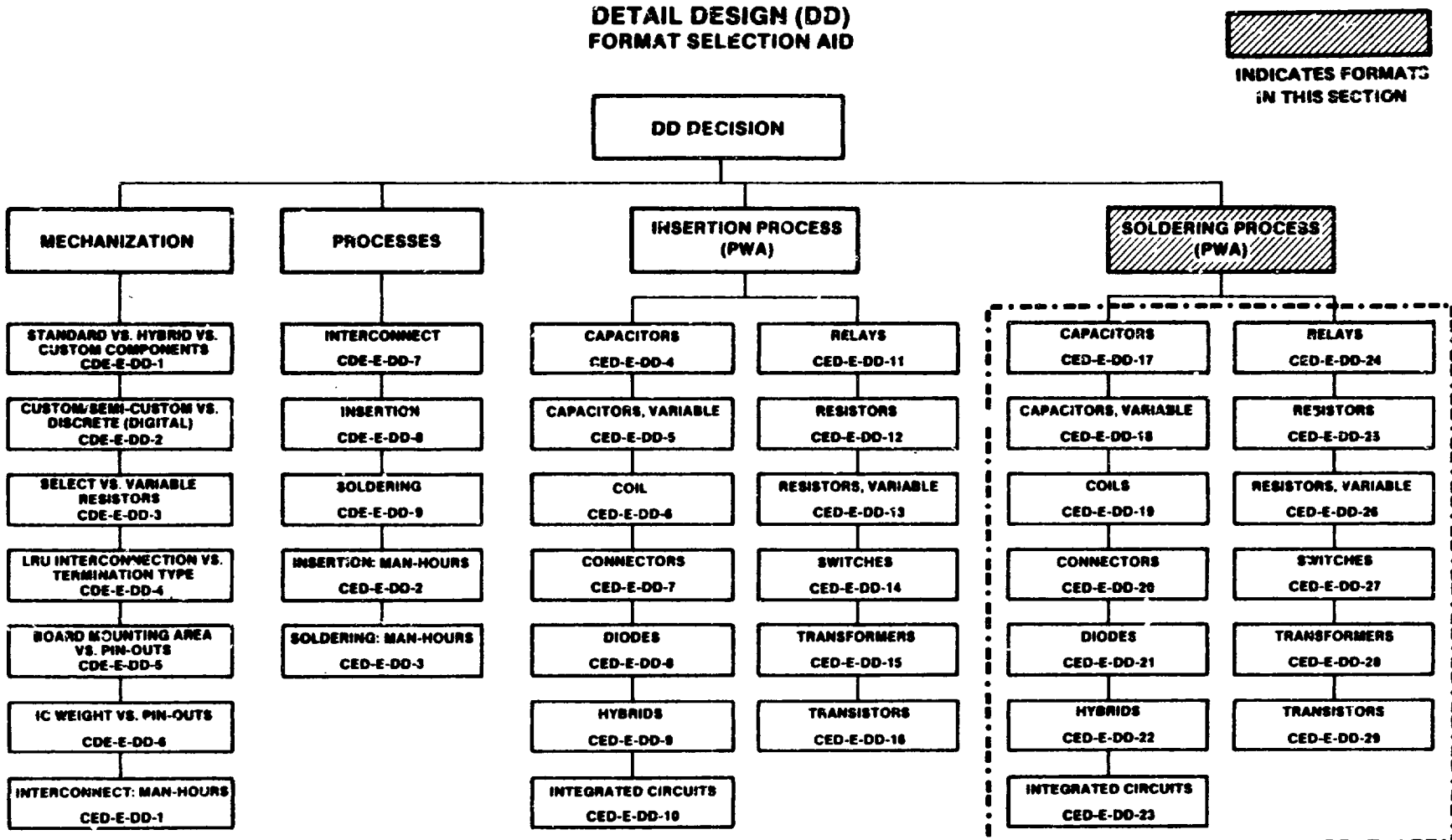
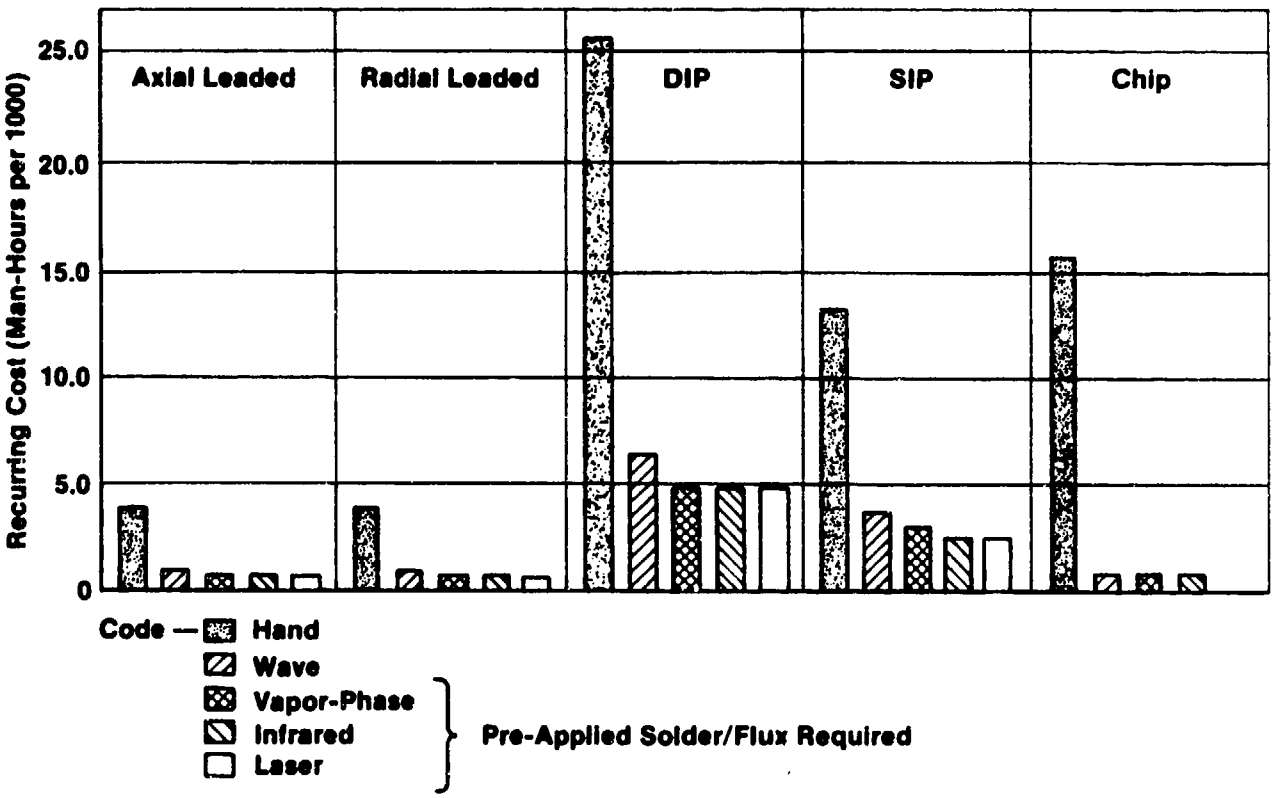


FIGURE 5-9. DETAIL DESIGN FORMAT SELECTION AID

FTR45026200U
3 Jan 1983

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)

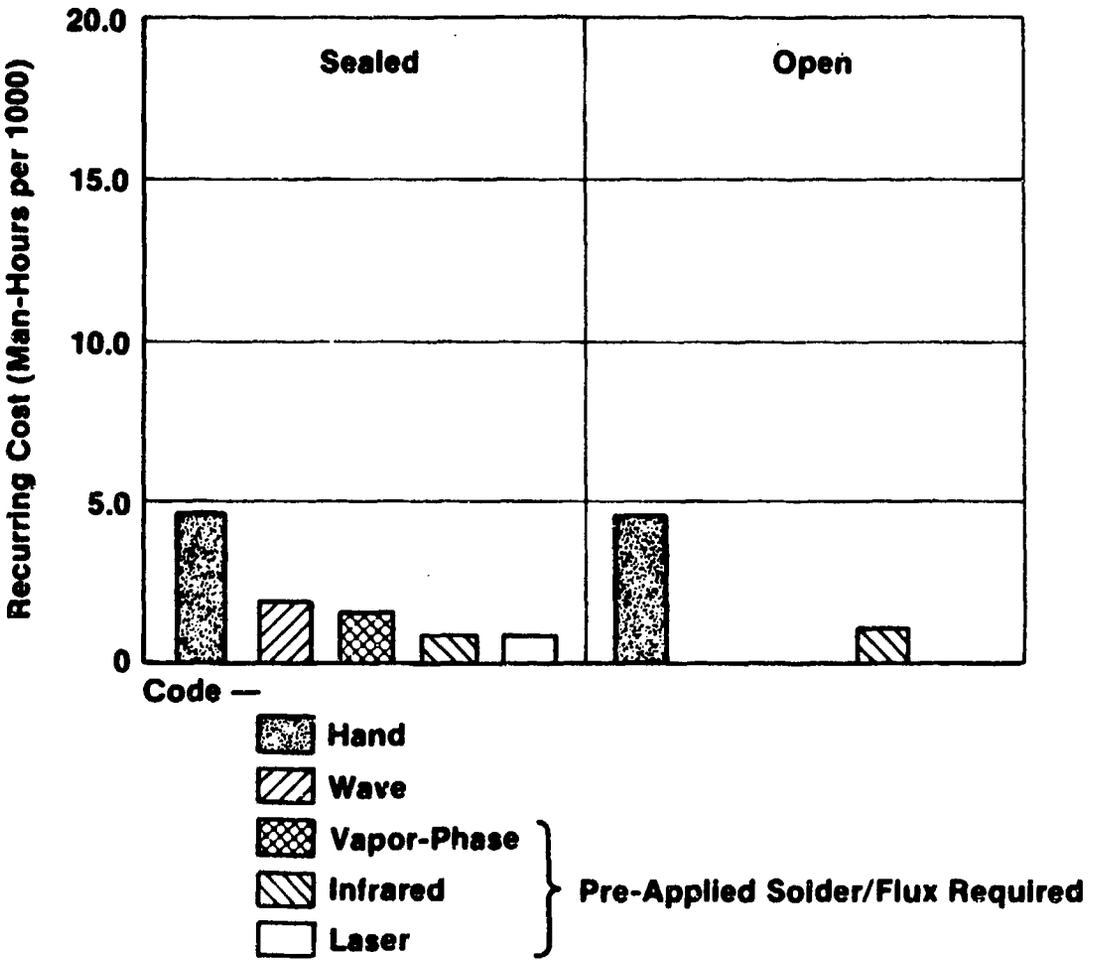
CAPACITORS



CED-E-DD-17

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)

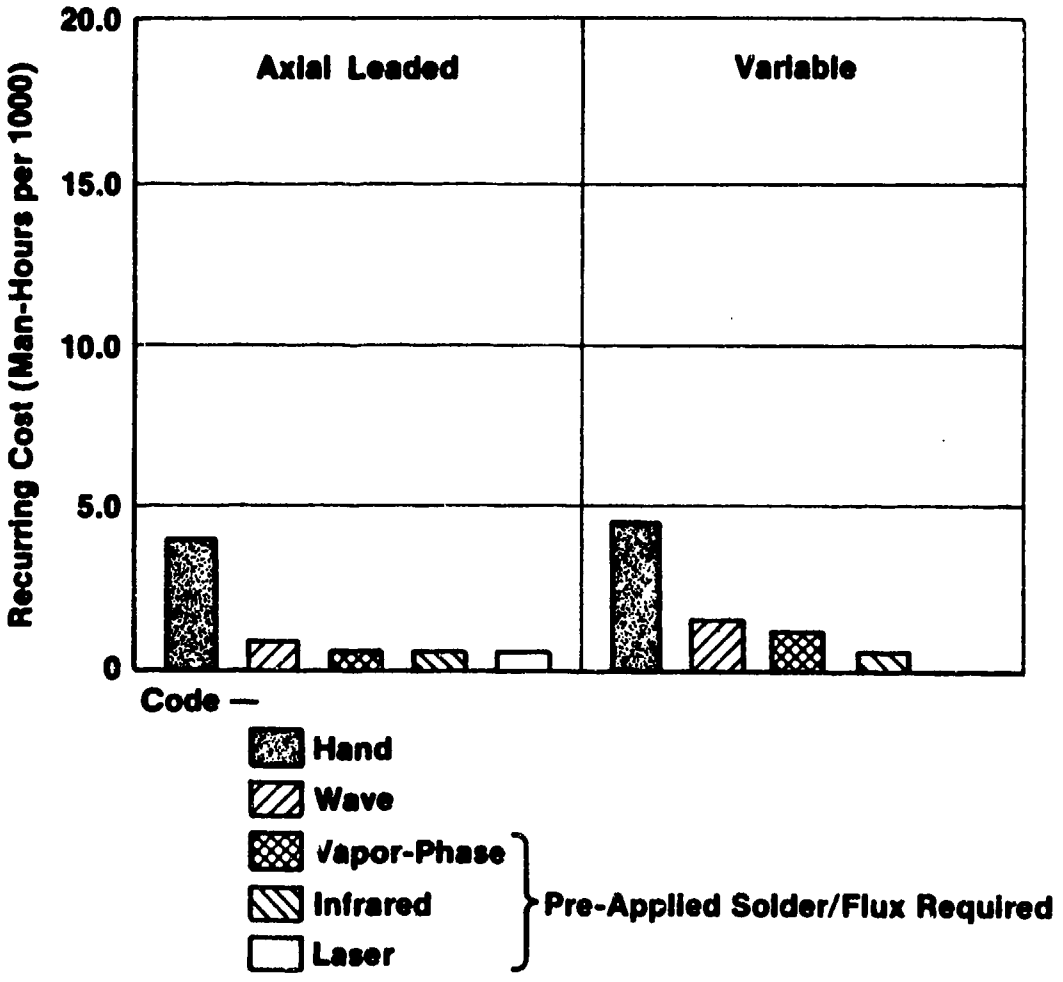
CAPACITORS, VARIABLE



CED-E-DD-18

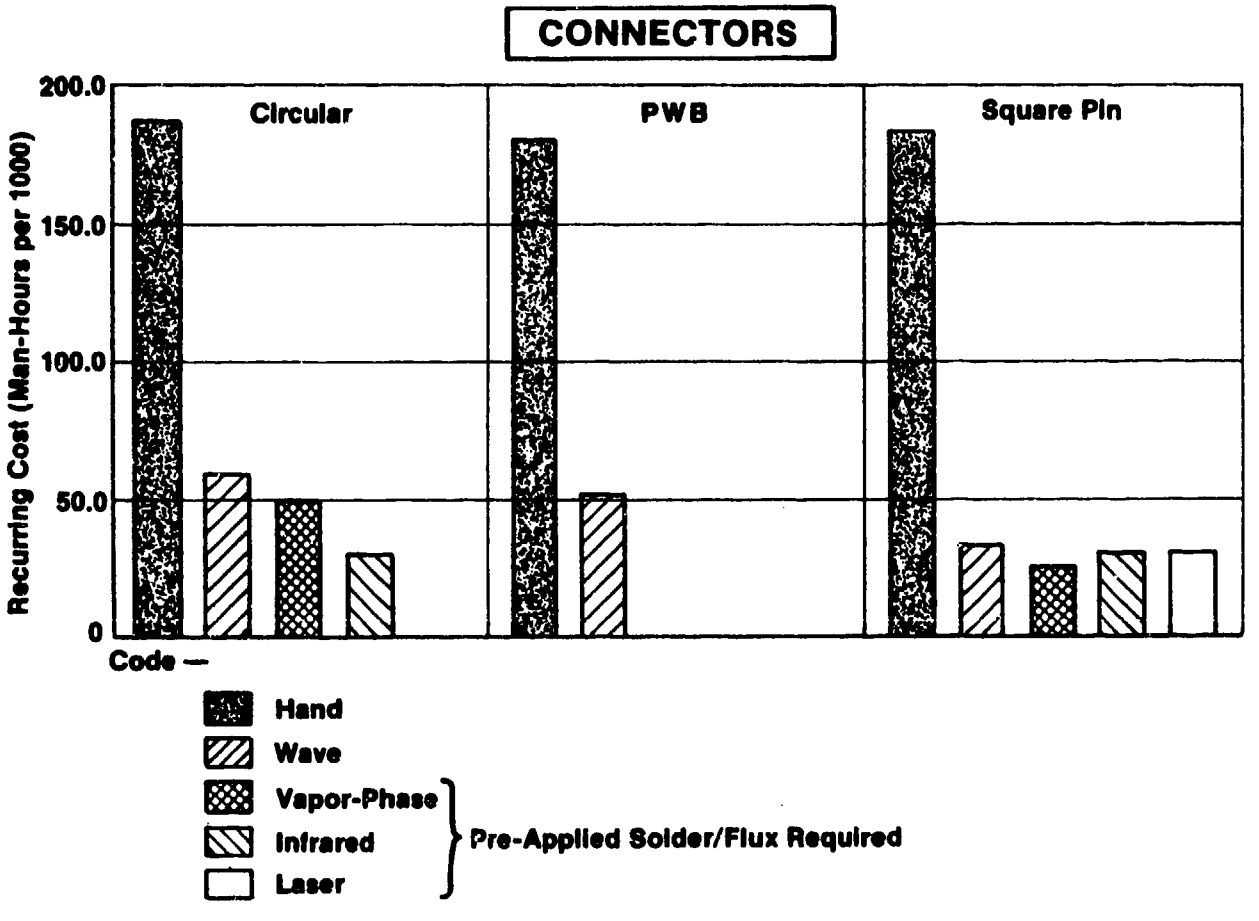
SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)

COILS



CED-E-DD-19

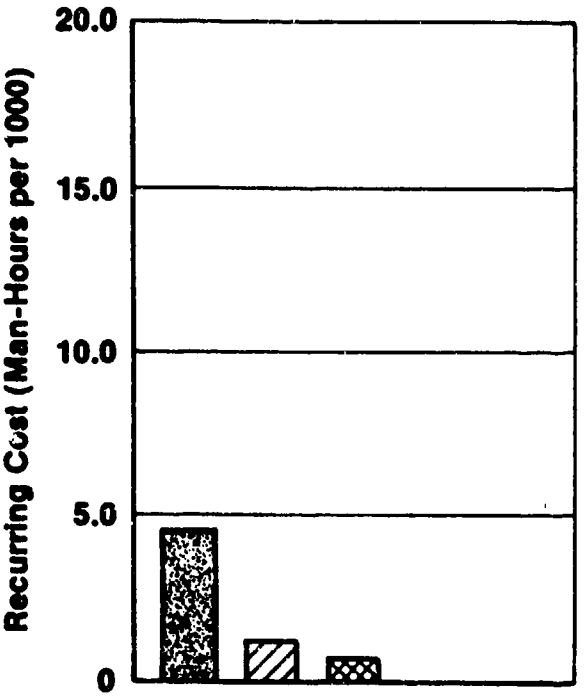
SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)



CED-E-DD-20

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)

DIODES



Code —

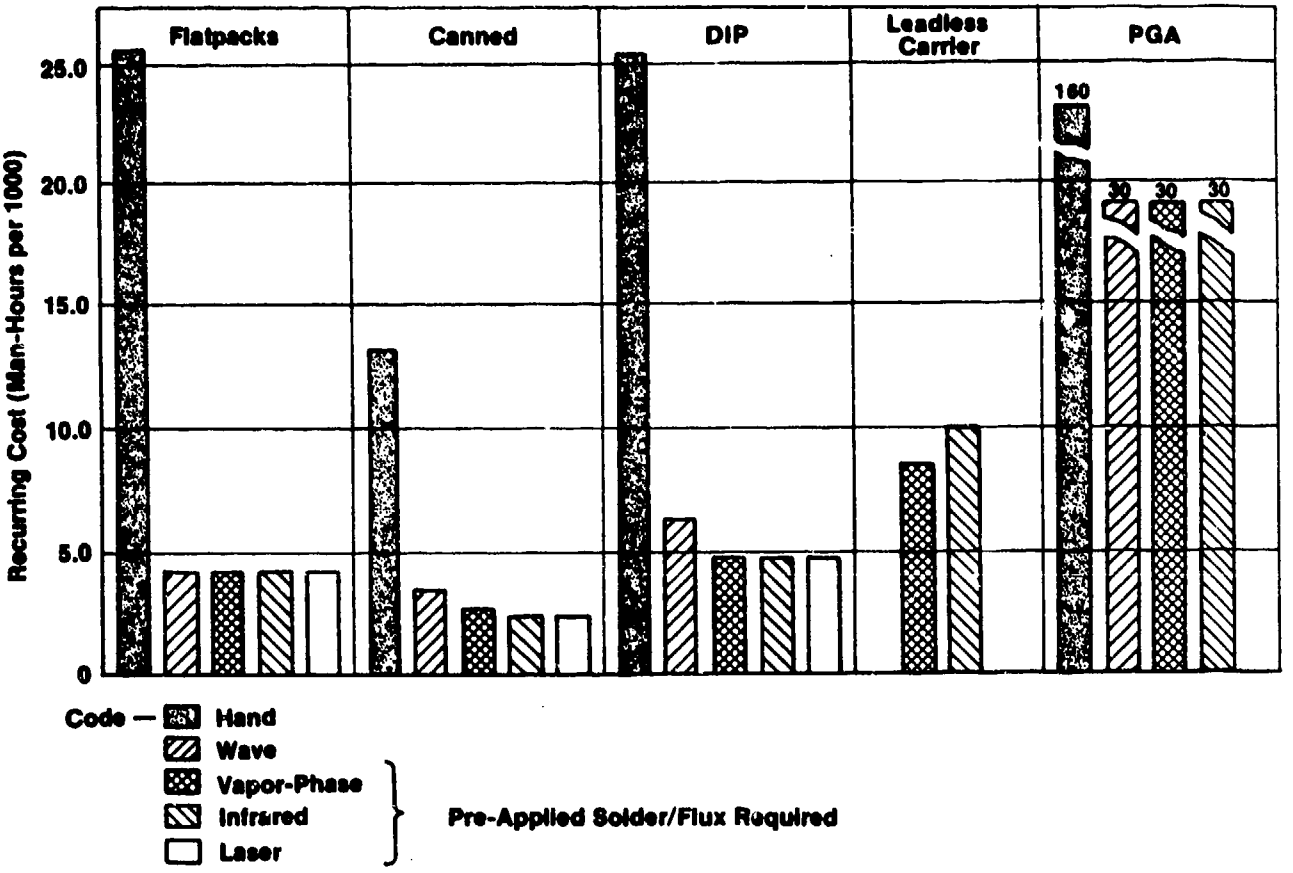
- Hand
- Wave
- Vapor-Phase
- Infrared
- Laser

} Pre-Applied Solder/Flux Required

CED-E-DD-21

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)

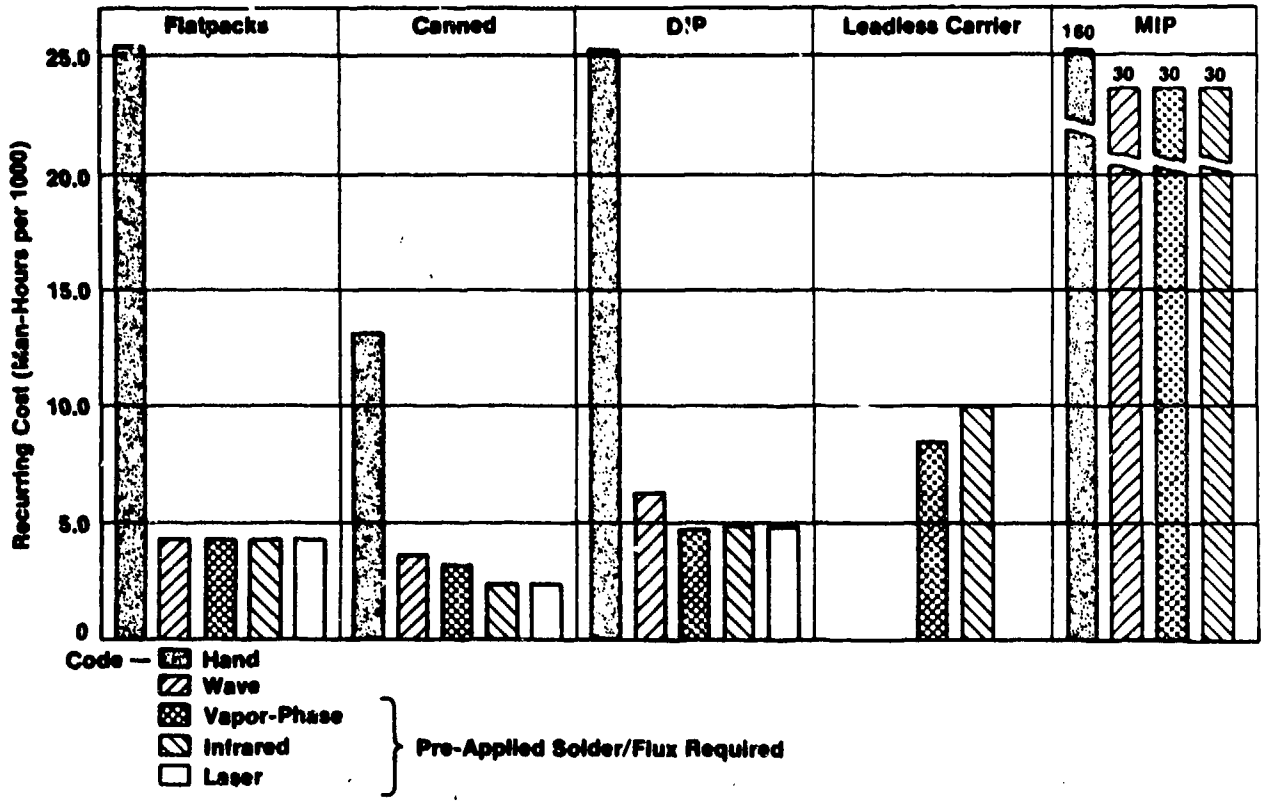
HYBRIDS



CED-E-DD-22

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)

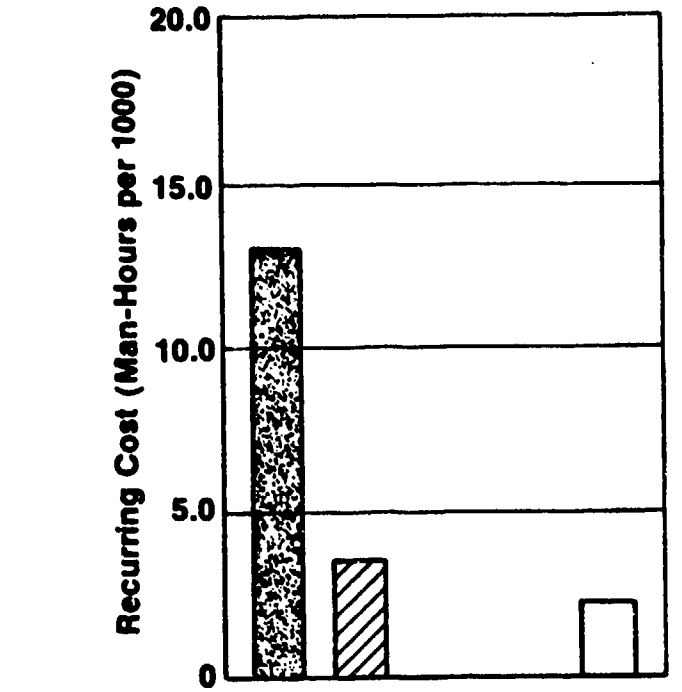
INTEGRATED CIRCUITS



CED-E-DD-23

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)

RELAYS



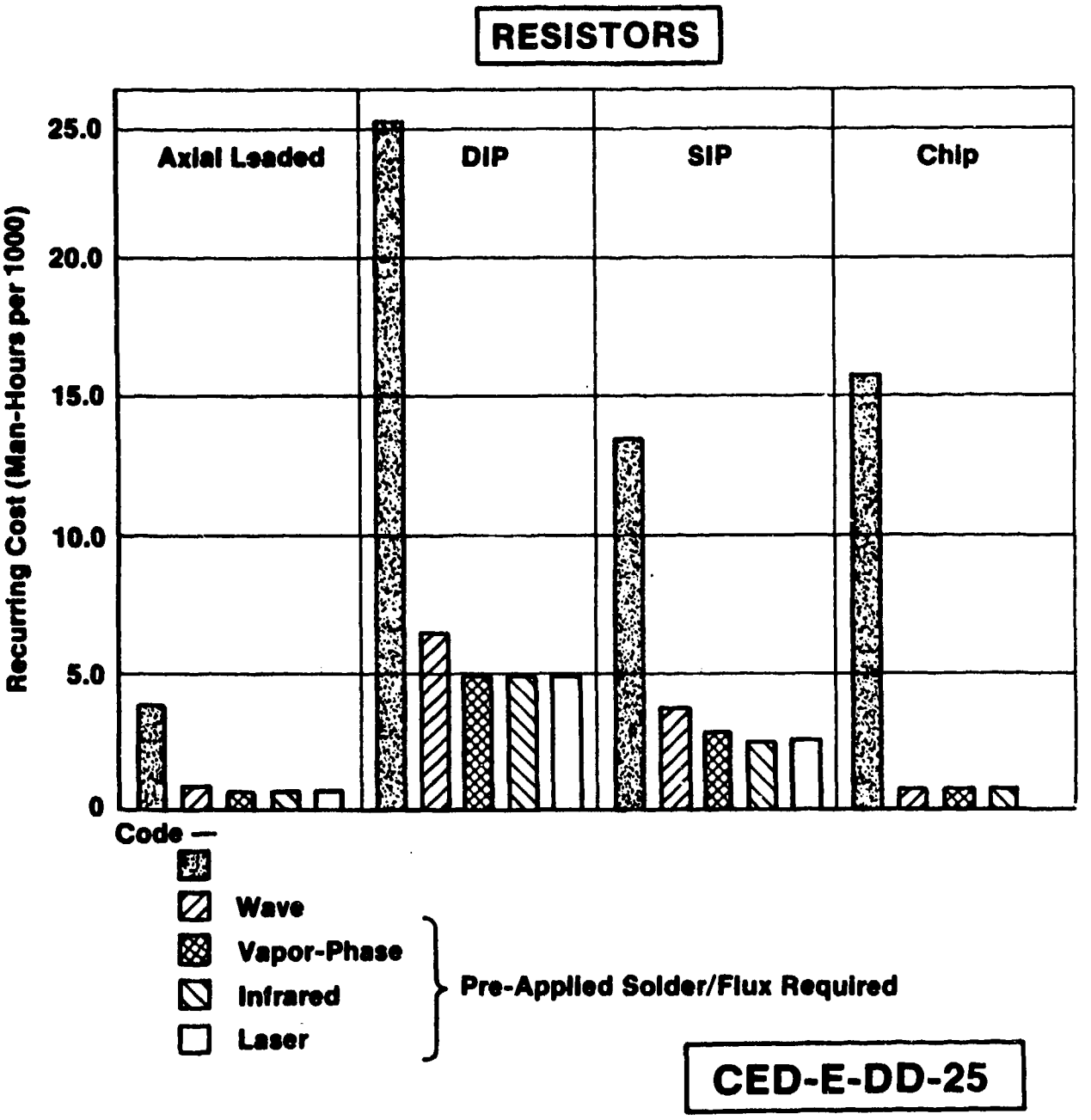
Code —

- Hand
- Wave
- Vapor-Phase
- Infrared
- Laser

} Pre-Applied Solder/Flux Required

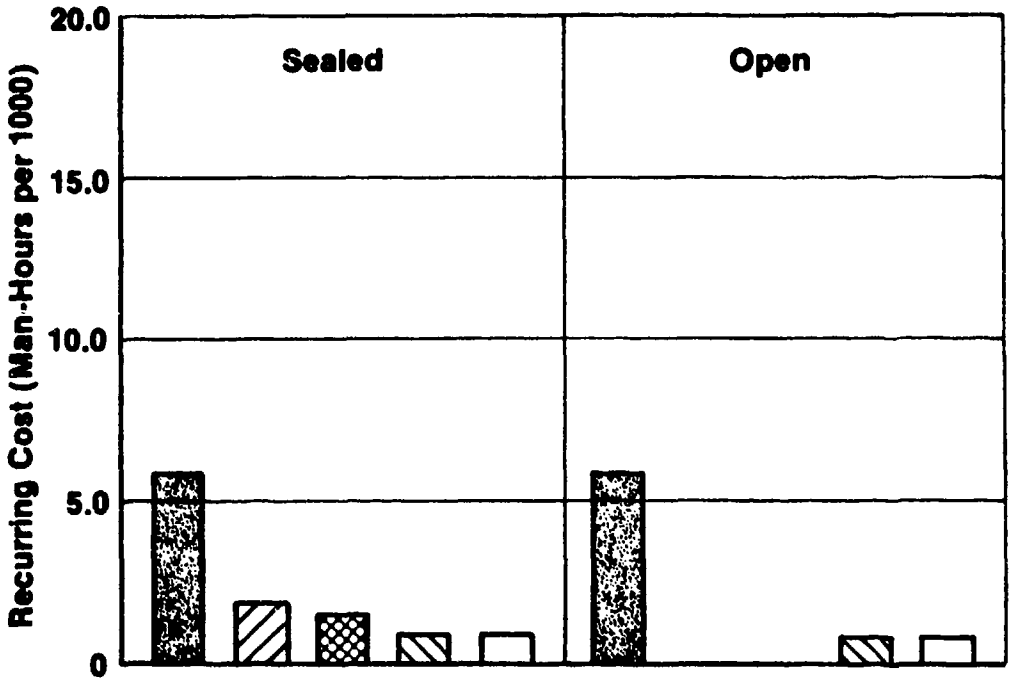
CED-E-DD-24

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)



SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)

RESISTORS, VARIABLE



Code —

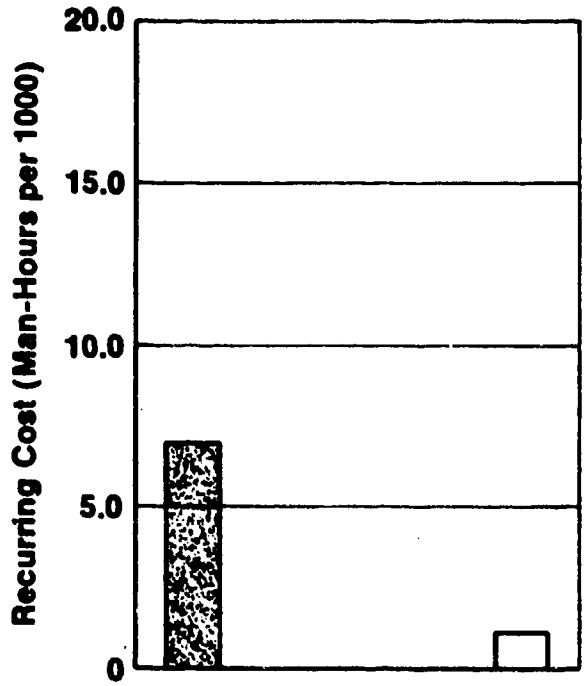
- Hand
- Wave
- Vapor-Phase
- Infrared
- Laser

} Pre-Applied Solder/Flux Required

CED-E-DD-26

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)

SWITCHES



Code —

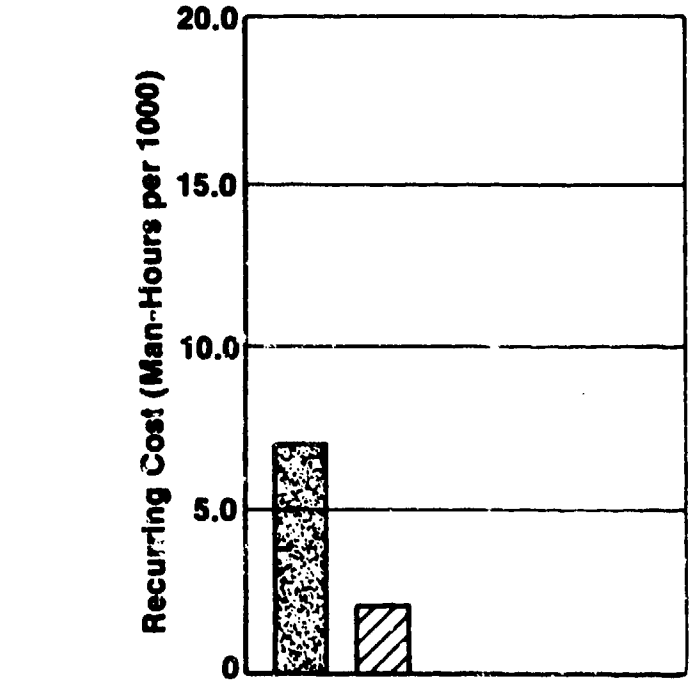
- Hand
- Wave
- Vapor-Phase
- Infrared
- Laser

} Pre-Applied Solder/Flux Required

CED-E-DD-27

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)

TRANSFORMERS



Code —

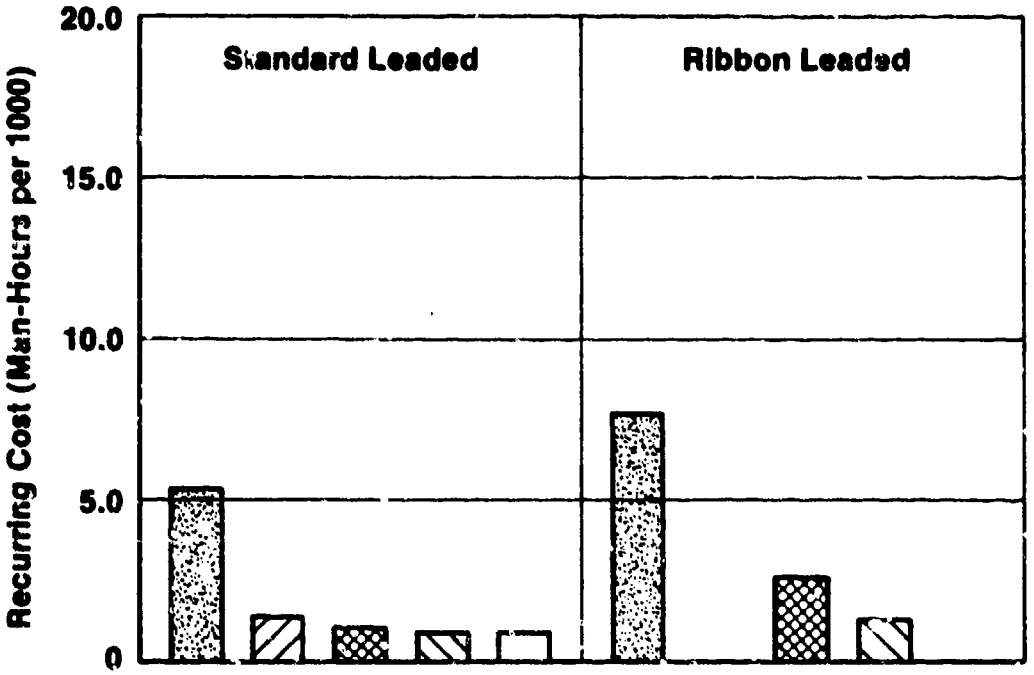
- Hand
- Wave
- Vapor-Phase
- Infrared
- Laser

} Pre-Applied Solder/Flux Required

CED-E-DD-28

SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)

TRANSISTORS



Code —

- Hand
- Wave
- Vapor-Phase
- Infrared
- Laser

} Pre-Applied Solder/Flux Required

CED-E-DD-29

SECTION 6
GROUND RULES FOR ELECTRONICS

Prior to the development of manufacturing cost data, it is necessary to establish both general and detailed ground rules. Ground rules are necessary and important because they promote understanding and ensure consistency, uniformity, and accuracy in generating and integrating data into the formats.

6.1 General Ground Rules

The general ground rules are categorized under the following major groupings:

- Electronic Assemblies
- Discrete Parts
- Materials
- Manufacturing Methods
- Facilities
- Data Generation - Recurring Costs
- Data Generation - Nonrecurring Costs
- Support Function Modifiers
- Test, Inspection, and Evaluation (TI&E).

6.1.1 Electronic Assemblies

(1) The electronic assemblies selected are those commonly used in the electronics industry. Examples of assemblies are printed wiring assemblies, power supplies, hybrids, cables, and chassis.

6.1.2 Discrete Parts

(1) The discrete parts selected are those commonly used in the aerospace electronics industry such as printed wiring board, wire, substrate, and connectors.

6.1.3 Materials

(1) The materials selected for the electronic assemblies are representative of the range of those more commonly used by industry.

(2) Material costs are included at the point of usage.

(3) Material costs of nonrecurring tooling are not included.

6.1.4 Manufacturing Methods

(1) Only existing manufacturing methods required to produce the base parts are considered. No emerging manufacturing methods are evaluated. However, the potential of new technologies to reduce costs are highlighted in the MC/DG.

(2) A production, in contrast to a prototype, environment is assumed.

(3) Manufacturing man-hour data are developed, where possible, for more than one manufacturing method for each discrete part or assembly. The data will thereby enable the designer using the MC/DG, with applicable utilization factors, to determine the most cost-competitive manufacturing method in trade-off studies.

(4) To generate an effective data base for each selected part, a factory operational sequence for each applicable manufacturing method has been established reflecting the most economical means of fabrication. This standardized sequence is used by each team member to determine the part cost in man-hours.

(5) Tools required to manufacture the various parts were identified on the data collection forms.

6.1.5 Facilities

(1) Only present manufacturing facilities, available to the electronics industry, were considered.

6.1.6 Data Generation - Recurring Costs

(1) All manufacturing labor-cost data are presented in man-hours and all material costs in vendor dollars.

(2) Electronic assembly labor cost is determined at unit 200 and based on team member learning curves.

(3) In developing data, each participating company utilized its own proprietary learning curves which will not be disclosed at BCL or the Air Force.

(4) The base part cost (man-hours/vendor dollars) is generated for each part type.

(5) Man-hour data were generated for all manufacturing operational sequences in part fabrication and assembly and include all hands-on factory direct labor operations prior to entering storage for subsequent assembly.

(6) Setup time (man-hours) is amortized over the selected lot size and added to the processing time to obtain the base part cost man-hours.

(7) Recurring tooling costs (tool maintenance, planning, etc.) are not included.

(8) Lot sizes to be considered for electronic assemblies were determined. The standard lot size selected was 20 assemblies.

(9) Procured item costs are based on company purchase order agreements.

(10) The part cost (man-hours/vendor dollars), as derived by each electronics company, was synthesized and normalized by BCL to reflect an industry team average for each base part, designer-influenced cost element (DICE), and discrete part.

(11) For proprietary reasons, realization factors including personal, fatigue, and delay (PF&D) standard hours and other business sensitive information employed at team member companies, were not included in the analysis or on the data sheets or designer-oriented formats in the "MC/DG for Electronics".

(12) No data provided by any team member will be disclosed by BCL to other team members, agencies, or to the public without the expressed approval of the team members participating in the program on the "MC/DG for Electronics".

6.1.7 Data Generation - Nonrecurring Costs

(1) Tool costs (man-hours) were generated for each fabricated part type. In addition, tool design and tool planning hours were evaluated with respect to their impact, to determine whether they should be included or omitted.

(2) The costs of production tooling, if included, were restricted to contract or project tools only. Standard test equipment costs were not included.

(3) Nonrecurring vendor costs (dollars) were included and amortized over the selected lot size.

(4) Special test equipment (STE) (i.e., fixtures, adapters, etc.) nonrecurring costs (man-hours/vendor dollars) were included and amortized over the selected lot size.

(5) Test software costs (man-hours) were considered as nonrecurring costs and amortized over the selected lot size.

(6) Nonrecurring tooling costs (NRTC) generated by the team companies were normalized by BCL for presentation in the "MC/DG for Electronics".

6.1.8 Support Function Modifiers

(1) Additional efforts other than factory labor, such as production control, industrial engineering, and manufacturing engineering were excluded from the part cost data supplied to BCL. These modifiers may be included later by the MC/DG users.

(2) Impact on manufacturing cost of reliability, maintainability, and life-cycle cost requirements included in product specifications will be identified for the various manufacturing method alternatives.

6.1.9 Test, Inspection, and Evaluation (TI&E)

(1) TI&E cost data (man-hours), were developed and then synthesized and normalized by BCL for "in-process, functional", and "final acceptance" inspection/testing.

6.2 Detailed Ground Rules

The detailed ground rules are categorized under the following major groupings:

- Material (Purchased Items)
- Configuration
- Specification Requirements
- Manufacturing Methods
- Facilities
- Test, Inspection, and Evaluation (TI&E)
- Data Generation - Recurring
- Data Generation - Nonrecurring.

6.2.1 Material (Purchased Items)

(1) All purchased parts are "off-the-shelf" standard parts.

(2) Parts consist of integrated circuits (DIP packages), resistors, capacitors, diodes, connectors, extractor(s), etc.

(3) The printed wiring board (PWB) is a purchased item.

(4) No purchased tooling is included.

6.2.2 Configuration

(1) The PWB is square with a surface area of 36 $in.^2$ (6 in. by 6 in.).

(2) The electronic part count is 75 pieces.

(3) The PWB is four-layer, G-10 (MIL-P-18177) board material, with 874 plated-through holes.

(4) Five cuts and jumpers are used.

6.2.3 Specification Requirements

(1) Military standards apply to part selection, quality, and workmanship practices.

(2) No assembly level screening.

6.2.4 Manufacturing Methods

(1) Ninety to one hundred percent of the parts are compatible with automatic insertion, and where economically feasible, are auto-inserted.
(2) The board is assumed to be wave-soldered with the appropriate masking performed.
(3) The cleaning procedure includes vapor degreasing or water wash.
(4) Part locations and assembly identifiers may be silk-screened.
(5) Conformal coating is applied using standard company practices.

6.2.5 Facilities

(1) Existing production facilities are evaluated when developing manufacturing man-hour data.

6.2.6 Test, Inspection, and Evaluation (TI&E)

(1) Company purchased part incoming inspection procedures are employed.
(2) In-circuit testing is conducted at the assembly level prior to any functional testing.
(3) Functional testing uses automatic procedures.
(4) Normal company inspection procedures are followed in complying with military standards.
(5) A 100 percent yield is assumed.

6.2.7 Data Generation - Recurring

(1) The lot sizes selected were 5, 10, and 25 assemblies.
(2) Purchased part costs were based on normal leadtimes and release quantities for production for 1 year.
(3) Company standard hours less personal, fatigue and delay (PF&D) were used.

6.2.8 Data Generation - Nonrecurring

(1) The in-circuit testing adapter costs were identified.

(2) Costs for special test equipment were identified.

(3) Software costs for in-circuit testing and automatic functional testing were identified.

SECTION 7
SUPPLEMENTARY FORMS

7.1 Supplementary Forms for Designer Use

To conveniently utilize the qualitative and quantitative manufacturing data presented in the "MC/DG for Electronics" for trade-off studies, various worksheets and formats appear in sections of this volume. These worksheets and formats have also been utilized in examples to illustrate their use.

While the use of the designer worksheets and certain formats in conceptual design is optional, a blank copy of each is included for the convenience of those who prefer this approach and would like to reproduce a supply. The copies included are:

Sheet 1: Conceptual Design Format Selection Chart

Sheet 2: Impact of New Technology Format

Sheet 3: Impact of Commonality Format

Sheet 4: Electronic Designer's Cost Worksheet

Sheet 5: Material Cost Worksheet

Sheet 6: Insertion Labor Estimation Worksheet (2 pages)

Sheet 7: Soldering Labor Estimation Worksheet (2 pages).

7.2 Document Request Order Form

The documents available on the ICAM "Manufacturing Cost/Design Guide" project are listed on the Request Order Form provided at the conclusion of this section (page 7-11). Note that all documents prepared under the contract have a controlled distribution and contain export control clauses.

Sheet 1

CONCEPTUAL DESIGN PHASE TRADE-OFFS
DESIGN PARAMETERS REQUIRED

System Design Parameters	Parameter Value (Specified or Developed)	Impact of: New Technology I	Number of Assemblies II	Common Functions III	Digital Design IV	Built-In Test V	Part Count VI
1. Reliability		●	●	●	×	●	●
2. Maintainability		●	×	○	×	●	×
3. Environmental		○	●	○	×	○	×
4. Part Costs		○	×	○	×	×	○
5. Test Cost		●	×	×	×	●	●
6. Assembly Cost		●	×	×	×	×	●
7. Factory Special Handling		●	○	○	○	○	●
8. Part Density		●	×	●	×	○	●
9. Number of Functions		○	○	○	●	×	○
10. Partitioning, Functional		×	●	×	●	×	×
11. Interface (With Other System)		×	●	●	●	×	×
12. Redundancy		×	●	×	●	●	×
13. Maintenance Concept		×	●	○	×	●	○
14. Aircraft Configuration		○	●	×	×	●	○
15. Fault Isolation		×	×	●	●	●	×
16. Mission Length		○	○	●	○	○	○
17. Vulnerability Levels		○	●	×	×	×	×

Parameters Required for Use of CDE Formats I-VI

● = Required Data
○ = Secondary Data
× = Not Used

Designer: _____
Date: _____

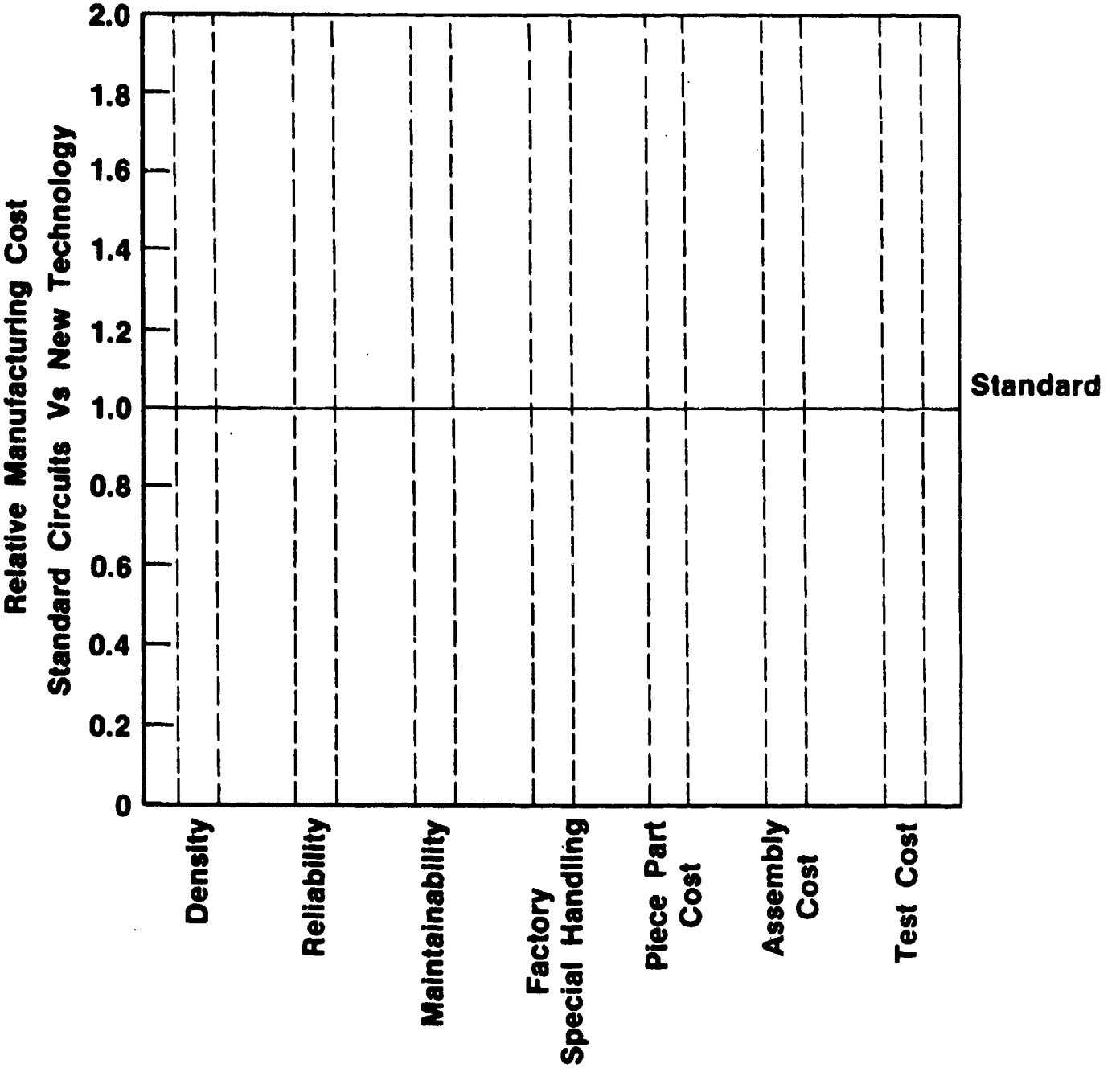
Sheet 2

IMPACT OF NEW TECHNOLOGY

New Technology: _____

Indenture Level: _____

Assembly Function: _____



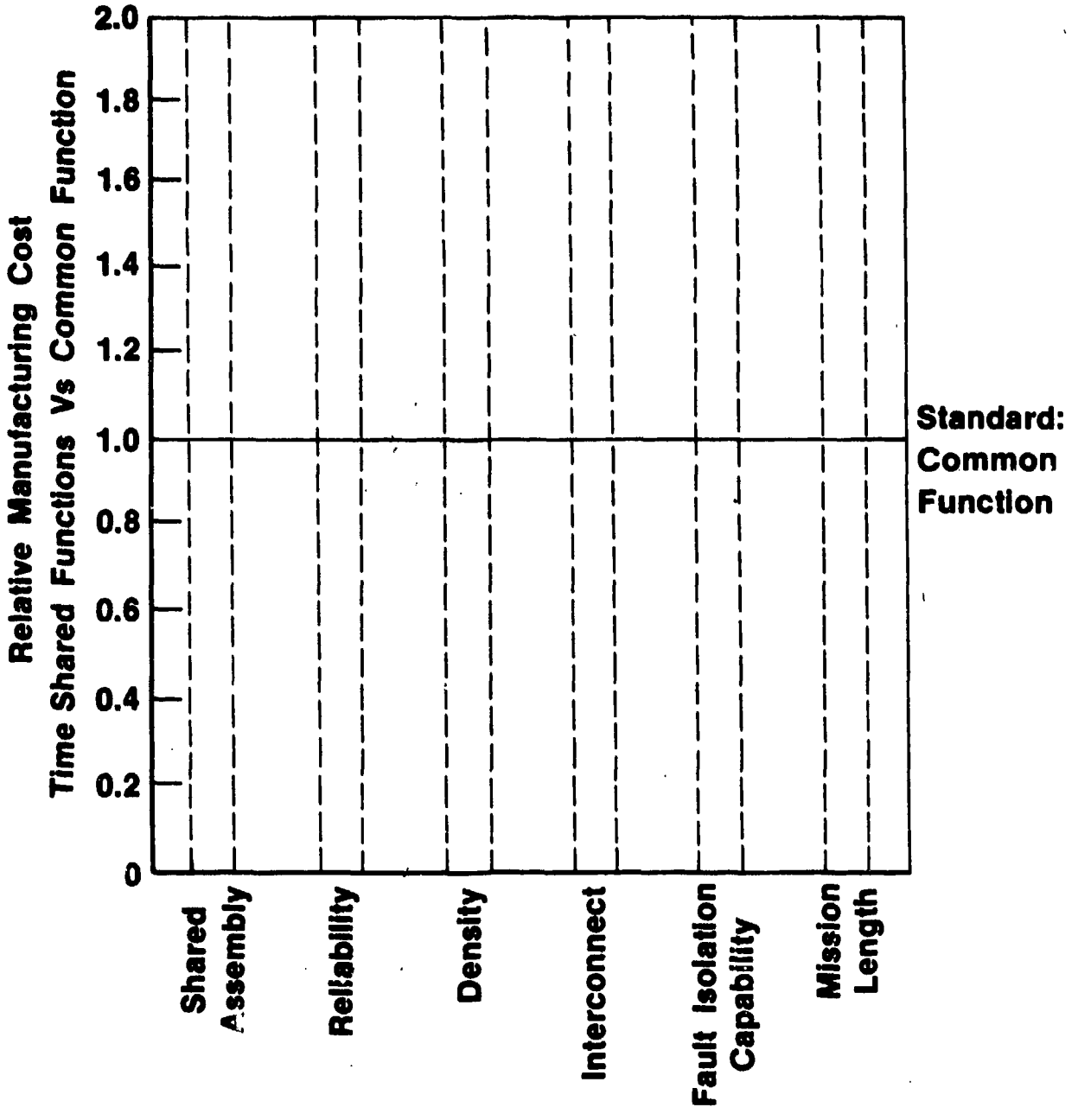
CDE-E-CD-I

Sheet 3

IMPACT OF COMMONALITY

Trade-Off Study: _____

Indenture Level: _____



CDE-E-CD-III

Sheet 4

MC/DG ELECTRONIC DESIGNER'S COST WORKSHEET

Baseline Configuration:
Indenture Level:

Baseline Manufacturing Cost Allocation: $ _____

DESIGN DECISION: Part Selection	1	2	3	4	5	6	7
Piece Part Type	**% Total Electronic Part Cost**	**Baseline Approach**	**Reference**	**Study Approach**	**Ratio: Baseline to Study Approaches**	**Cost Factor (%) (1 ÷ 5)**	**Cost* Change (%) (1 - 6)**

Total _____

Cost Impact: **Baseline Manufacturing Cost ($) x Cost Change Total (%) = ($)** _____ **x** _____ **(%: Total of Column 7) = ($)** _____

New Cost: **Baseline Manufacturing Cost ($) - Cost Impact = ($)** _____ **-($)** _____ **= ($)** _____

***Notes:** **Positive Value = Cost Savings**
Negative Value = Cost Increase

Remarks _____

_____

By: _____

Date: _____

FTR450262UUU
3 Jan 1983

Sheet 5

MATERIAL WORKSHEET

ICAM "MANUFACTURING COST/DESIGN GUIDE (MC/DG)" FOR ELECTRONICS AND FABRICATION ASSEMBLY

ASSEMBLY TYPE:_____ **LOT SIZE:**_____

VENDOR PART NUMBER	PART DESCRIPTION	QUANTITY PER ASSEMBLY	PACKAGE TYPE	COST $/PART	NON-RECURRING VENDOR COST/MAN HOURS	RECURRING COST $/ASSEMBLY	% OF TOTAL COST
SUMMATION							100.0

FTR45026200OU
3 Jan 1983

Sheet 6

INSERTION LABOR ESTIMATION WORKSHEET

ASSEMBLY NAME: _____ **SHEET 1 OF 2**

	COLUMN			1	2		
	INSERTION PROCESS				PROCESS ALTERNATIVES		
	MAN-HOURS PER 1000				EXTENDED MAN-HOURS PER 1000		
PART TYPE	AUTO	SEMI-AUTO	HAND	QUANTITY PER ASSEMBLY	AUTO	SEMI-AUTO	HAND
RESISTORS							
Axial-Leaded	0.29	2.39	2.94				
DIP	0.44	4.44	4.74				
SIP	N/A	3.00	3.34				
Chip	0.47	1.20	2.10				
VARIABLE RESISTORS							
Sealed	N/A	4.00	4.59				
Open	N/A	4.00	4.59				
CAPACITORS							
Axial Leaded	0.29	2.39	2.04				
Radial Leaded	0.29	2.89	3.14				
DIP	0.44	4.40	4.74				
SIP	N/A	3.00	3.34				
Chip	0.47	1.20	2.10				
VARIABLE CAPACITORS							
Sealed	N/A	2.34	2.59				
Open	N/A	2.34	2.59				
COILS							
Axial Leaded	0.25	2.39	2.94				
Variable	N/A	N/A	2.50				
DIODES	0.25	1.83	2.33				
	SHEET 1 SUMMATION						
	PROCESS ALTERNATIVES				AUTO	SEMI-AUTO	HAND

Sheet 6
(Continued)

INSERTION LABOR ESTIMATION WORKSHEET (Continued)

ASSEMBLY NAME: _____ **SHEET 2 OF 2**

	COLUMN			1	2		
	INSERTION PROCESS				PROCESS ALTERNATIVES		
	MAN-HOURS PER 1000				EXTENDED MAN-HOURS PER 1000		
PART TYPE	AUTO	SEMI-AUTO	HAND	QUANTITY PER ASSEMBLY	AUTO	SEMI-AUTO	HAND
TRANSISTORS							
Standard Leaded	N/A	3.74	4.20				
Ribbon Leaded	N/A	N/A	7.83				
INTEGRATED CIRCUIT							
Flatpacks	N/A	5.80	4.32				
Canned	N/A	6.95	7.84				
DIP	0.44	4.40	4.74				
Leadless Carrier	0.55	8.00	7.67				
MIP							
HYBRIDS							
Flatpacks	N/A	5.80	4.32				
Canned	N/A	6.95	7.84				
DIP	0.44	4.40	4.74				
Leadless Carrier							
SWITCHES	N/A	N/A	4.37				
TRANSFORMERS	N/A	N/A	5.17				
RELAYS	N/A	N/A	5.07				
CONNECTORS (100 PIN)							
Circular	N/A	N/A	118.35				
Printed Circuit	N/A	N/A	79.75				
Square Pin	13.33	60.00	86.65				
	SHEET 2 SUMMATION						
	SHEET 1 SUMMATION						
	TOTAL SUMMATION						
	PROCESS ALTERNATIVES				AUTO	SEMI-AUTO	HAND

Sheet 7

SOLDERING LABOR ESTIMATION WORKSHEET

ASSEMBLY NAME: _____ **SHEET 1 OF 2**

	COLUMN					1	2				
	SOLDERING PROCESS						PROCESS ALTERNATIVES				
	MAN-HOURS PER 1000						EXTENDED MAN-HOURS PER 1000				
PART TYPE	H	W	Vϕ	IR	L	QUANTITY PER ASSEMBLY	H	W	Vϕ	IR	L
RESISTORS											
Axial-Leaded	3.90	0.84	0.64	0.60	0.60						
DIP	25.32	6.33	4.79	4.80	4.80						
SIP	13.18	3.57	2.75	2.40	2.40						
Chip	15.54	0.60	0.65	0.60	N/A						
VARIABLE RESISTORS											
Sealed	5.88	1.88	1.57	0.90	0.90						
Open	5.88	N/A	N/A	0.90	0.90						
CAPACITORS											
Axial-Leaded	3.90	0.84	0.64	0.60	0.60						
Radial Leaded	3.90	0.84	0.64	0.60	0.60						
DIP	25.32	6.33	4.79	4.80	4.80						
SIP	13.18	3.57	2.75	2.40	2.40						
Chip	15.54	0.60	0.65	0.60	N/A						
VARIABLE CAPACITORS											
Sealed	4.70	1.88	1.57	0.90	0.90						
Open	4.60	N/A	N/A	0.90	N/A						
COILS											
Axial-Leaded	3.90	0.84	0.64	0.60	0.60						
Variable	4.67	1.50	1.19	0.60	N/A						
DIODES	4.60	1.08	0.67	N/A	N/A						
	SHEET 1 SUMMATION (ε)										
	PROCESS ALTERNATIVES						H	W	Vϕ	IR	L

Sheet 7
(Continued)

SOLDERING LABOR ESTIMATION WORKSHEET (Continued)

ASSEMBLY NAME:_____ SHEET 2 OF 2

	COLUMN					1	2				
	SOLDERING PROCESS						PROCESS ALTERNATIVES				
	MAN-HOURS PER 1000						EXTENDED MAN-HOURS PER 1000				
PART TYPE	H	W	Vφ	IR	L	QUANTITY PER ASSEMBLY	H	W	Vφ	IR	L
TRANSISTORS											
Standard Leaded	5.40	1.40	1.09	0.90	0.90						
Ribbon Leaded	7.71	N/A	2.62	1.30	N/A						
INTEGRATED CIRCUIT											
Flatpacks	25.67	4.20	4.20	4.20	4.20						
Canned	13.18	3.57	2.75	2.40	2.40						
DIP	25.32	6.33	4.79	4.80	4.80						
Leadless Carrier	N/A	N/A	8.54	10.00	N/A						
MIP											
HYBRIDS											
Flatpacks	25.67	4.20	4.20	4.20	4.20						
Canned	13.18	3.57	2.75	2.40	2.40						
DIP	25.32	6.33	4.79	4.80	4.80						
Leadless Carrier	N/A	N/A	8.54	10.00	N/A						
SWITCHES	6.96	N/A	N/A	N/A	1.20						
TRANSFORMERS	6.96	1.90	N/A	N/A	N/A						
RELAYS	13.18	3.57	N/A	N/A	2.40						
CONNECTORS (100 PIN)											
Circular	187.0	59.9	50.1	30.0	N/A						
Printed Circuit	178.1	51.0	N/A	N/A	N/A						
Square Pin	179.7	33.6	25.2	30.0	30.0						
SHEET 2 SUMMATION											
SHEET 1 SUMMATION											
TOTAL SUMMATION											
PROCESS ALTERNATIVES							H	W	Vφ	IR	L

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